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DESIGN OF PRECISION RSSI CIRCUIT FOR WIRELESS POWER
TRANSFER RECEIVERS

by

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American University of Sharjah
College of Engineering
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of the Requirements
for the Degree of

Master of Science in
Electrical Engineering

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Declaration of Authorship

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Dedication

To my family...

Abstract

Tracking systems for wireless power transfer (WPT) systems are becoming a necessity. WPT is a modern way of wirelessly charging devices using RF beams. The target signals are sometimes too weak to be received, which is why it is critical to have a dedicated received signal strength indicator (RSSI) at the receiver side for signal detection. It can also be used for transmitter localization and automatic gain control (AGC) to ensure continuous coverage. In this thesis, an RSSI coupled with a high-speed full-wave rectifier is designed to operate at 5.8 GHz. A sensitivity level of 10 uV, logarithmic error of 0.4 dB, and dynamic range of 34 dB are achieved by the proposed system. The proposed RSSI system is designed for a moving wireless power transfer receiver using TSMC 65 nm CMOS technology, and it is aimed at WPT systems that require high sensitivity.

Keywords: Wireless power transfer; WPT; received signal strength indicator; RSSI; Logarithmic; high sensitivity.

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List of Abbreviations

AGC	-	Automatic Gain Control
CMRR	-	Common-mode Rejection Ratio
FWR	-	Full-Wave Rectifier
LPF	-	Low Pass Filter
PSRR	-	Power-supply Rejection Ratio
RSSI	-	Received Signal Strength Indicator
SDLA	-	Successive Detection Logarithmic Amplifier
UAV	-	Unmanned Aerial Vehicle
WPT	-	Wireless Power Transfer

Chapter 1. Introduction

Wireless systems are continuously increasing, and hence the need for a system that would track the wireless device is increasing as well. A major example is the importance of tracking drones in the air that use wireless power transfer (WPT) transmitting RF beams as the charging topology. The signals received at the receiver have varying amplitudes which sometimes cause the desired signals to be too weak and below the receiver sensitivity level. Therefore, a received signal strength indicator (RSSI) is important for signal detection. RSSI systems are also used for automatic gain control (AGC) to ensure continuous coverage [1] or if the received power is too strong. The most recent wireless power transfer (WPT) method is to wirelessly charge devices using RF beams. To be able to track the signal's strength effectively while moving, it is very critical to have a high-precision RSSI system at the receiver side. The WPT aims to charge multiple drones moving in the air on a smart farm. In such a scenario, each drone, also known as unmanned aerial vehicle (UAV), needs to be equipped with an RSSI receiver system. This thesis proposes a logarithmic detector using 65 nm technology which acts as an RSSI system. Logarithmic detectors are a great choice for RSSI because of their fast impulse response and settling time. Also, logarithmic detectors, if designed effectively, can produce a linear-in-dB behavior which is ideal for signal detection because of its wide dynamic range. Another advantage of using logarithmic detectors is that they allow input power strength to be easily determined since the RSSI value can simply be multiplied by a certain factor or using a conversion table which can then be used for localization or AGC purposes. The proposed RSSI is designed for wireless power transfer receiver systems using TSMC 65 nm CMOS technology, works for 5G and 6G applications, and is aimed at WPT systems that require high sensitivity.

1.1. Thesis Objectives

UAVs used today are faced with a major challenge due to battery capacity that limits UAV flight duration. Contact-based conductive charging technique, the most popular charging method used in drones today requires extremely accurate alignment with the charging station, making it ineffective in harsh weather conditions. The UAV charging systems most used these days are costly and inefficient when operating on a large scale. UAVs, such as drones operating for smart farms that use IOT sensors to identify diseased plants, reduce water consumption, and identify humidity levels, should be able

to complete their job and automatically recharge quickly and in an efficient manner. Thus, WPT using RF beams is the most efficient charging topology for UAVs due to its long charging distance and operation in harsh weather conditions. Considering that UAE is highly investing in smart farming using clean energy, WPT using RF beams is ideal since it is an environment-friendly charging method. Thus, an RSSI circuit that will be placed in each drone is proposed which aims to successfully track and detect the WPT signals on air to ensure continuous drone charging and transmitter localization. It is also important to note that the proposed RSSI is suitable for 5G and 6G applications.

1.2. Research Contribution

The contributions of this research work can be summarized as follows:

- RSSI for WPT RF signal detection that is suitable for 5G and 6G applications without the use of downconverters
- An RSSI system with very high sensitivity
- The proposed RSSI accepts a very wide range of input frequencies

1.3. Thesis Organization

The rest of the thesis is organized as the following: Chapter 2 is the literature review which includes background about WPT and RSSI, in addition to the related work done in the RSSI field. Chapter 3 discusses the proposed work which consists of the proposed idea, RSSI system specification, and the proposed RSSI architecture. Moreover, Chapter 4 presents cadence virtuoso simulation results and results discussion. The last chapter, Chapter 5, provides a conclusion and outline for future work.

Chapter 2. Background and Literature Review

This chapter provides an overview of wireless power transfer and its different types. After understanding the necessity of wireless power transfer using RF beams, the received signal strength indicators (RSSI) and their significant importance for wireless signals detection are explained. This chapter also gives an overview of the RSSI functionality, shows a comparison between different RSSI topologies, and discusses the use of RSSI in transmitter localization. The literature review focuses on previous work that contributed to the RSSI field in different ways.

2.1. Introduction to Wireless Power Transfer

Wireless Power Transfer (WPT) is a technology that transmits power to electrical devices across an air gap. One of the most common uses of wireless power transfer is wireless charging. Wireless charging technology is continuously evolving in theory and application as it has significant benefits. The obvious benefit of this technology is that it is user-friendly as it doesn't require connecting cords. Other benefits include allowing for the fabrication of smaller devices and providing better durability since it can withstand harsher weather conditions and dust. Moreover, it also increases flexibility because, with wireless charging, the battery replacement process can be avoided. However, a wireless charging system costs more than wired charging implementation-wise because in addition to the wireless charger, a wireless power receiver must also be implanted on the device that needs to be charged.

Although wireless charging exists since the 1960s, only in the past two decades it has been of utmost importance due to the increasing use of portable devices. In recent years, the use of wireless charging has been on a rapid rise in many fields, especially in the field of smart technology [2]. Figure 2.1 shows the U.S. wireless charging market growth by application from the year 2012 to 2022 [3].

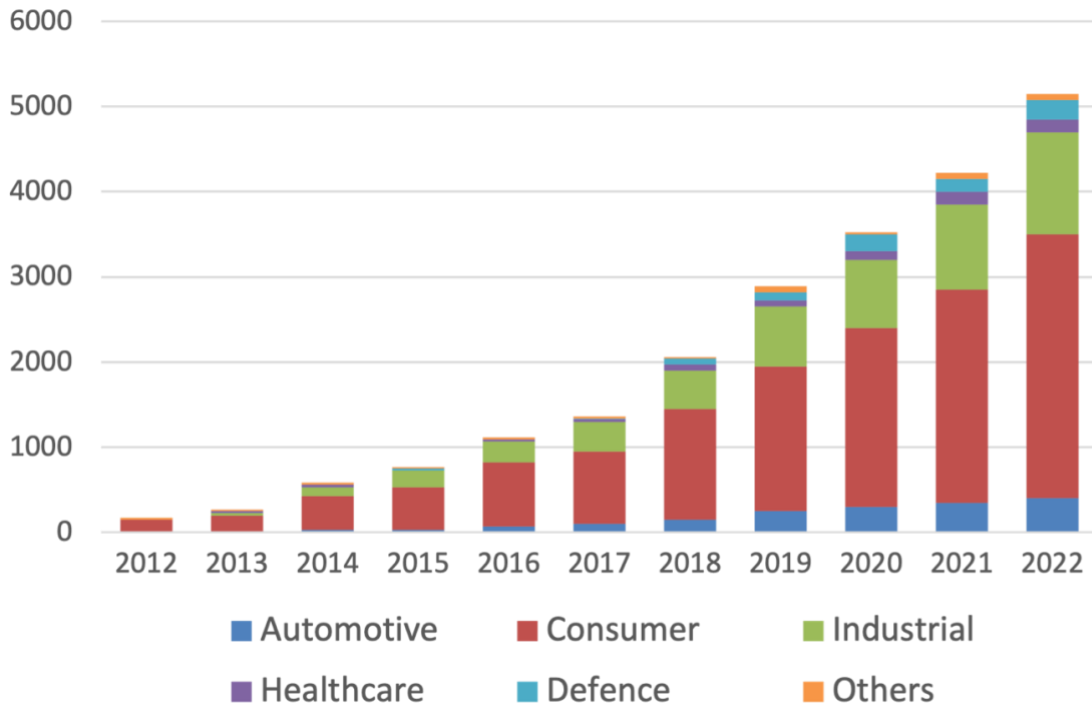


Figure 2. 1: U.S. wireless charging market by application from the year 2012 to 2022 (USD Million)

2.2. Fundamentals of Wireless Power Transfer

So far, the WPT technologies used are classified into radiative and nonradiative technology. Nonradiative technologies include inductive coupling, magnetic resonance coupling, and capacitive coupling. Radiative technologies are directive RF beamforming and nondirective RF power transfer. The limitation of capacitive coupling is that the coupling it can achieve depends on the available area of the device, which is difficult to accomplish for a typical portable device size. Regarding RF power beamforming, the obvious limitation is that it requires knowledge of the location of the receiver. Hence, the other WPT technologies are more commonly used. The RF power beamforming is the most suitable for our application since it provides a good amount of power in a directed area which can be identified with the help of the radar system [4].

2.2.1. Inductive coupling

Inductive coupling happens when magnetic induction allows the transfer of electrical energy between two coils. This will induce a voltage across the secondary coil where our target receiver will receive its energy from if within the field of the secondary coil which will wirelessly charge the device. To enhance the charging efficiency, the secondary coil must be tuned at the operating frequency. Usually, the effective charging

distance for this technology is within 20cm. The operating frequency is in kilohertz [4]

2.2.2. Magnetic resonance coupling

This technology is like inductive coupling in that both are based on the transfer of energy between two coils through magnetic induction. However, due to the resonance circuits, it can transfer power within a larger distance and can charge multiple devices simultaneously. The issue here is that interference occurs as a result of the mutual coupling of receiving coils. Thus, proper tuning is needed.

2.2.3. RF radiation

Frequency of RF ranges between 300MHz to 300GHz. The power transmission on the transmitter side starts with an AC-to-DC and then a DC-to-RF. This RF beam propagates till it reaches the receiver in which the RF is converted back to DC through an RF-to-DC converter. Microwaves can be used to deliver and transfer information at the same time. The useful band in this work lies in allowed ISM band frequencies. Their amplitude and phase are used for modulation so that the information can be sent, while their radiation and vibration are used to transfer energy used for charging. This is known as simultaneous wireless information and power transfer (SWIPT) [4].

Table 2.1 compares the different wireless charging techniques [4]. Wireless power transfer (WPT) using RF beams can be detected and tracked using a system on the receiver side called a received signal strength indicator (RSSI).

Table 2. 1: Comparison between different wireless charging techniques

Wireless charging technique	Advantage	Disadvantage	Effective charging distance
Inductive coupling	Safe for human, simple implementation	Short charging distance, heating effect, not suitable for mobile applications, needs tight alignment between chargers and charging devices	From a few millimeters to a few centimeters
Magnetic resonance coupling	Loose alignment between chargers and charging devices, charging multiple devices simultaneously on different power, high charging efficiency, non- line-of-sight charging	Not suitable for mobile applications, limited charging distance, complex implementation	From a few centimeters to a few meters
RF radiation	Long effective charging distance, suitable for mobile applications	Not safe when the RF density exposure is high, low charging efficiency, line- of-sight charging	Typically within several tens of meters, up to several kilometers

2.3. RSSI Background

Received signal strength indicator (RSSI) is a measure of the received signal's power level. The RSSI circuit presented in Figure 2.2 is based on successive detection architecture which is the most common architecture used for RSSI as shown in [1]. It consists of various limiting amplifiers having the same saturation voltage, a rectifier after each limiting amplifier, and a low pass filter (LPF) that results in a DC level of the input. However, it will only result in DC if the stop-band attenuation of the LPF is infinite which is not the case in practice. That is because to have an infinite stop-band attenuation or transition band, it requires the impulse response of the filter to be infinitely long and non-causal. The output of a non-causal system depends on inputs from the future which is not possible since a practical system cannot react to the future. Hence, there are always some ripples in the RSSI output.

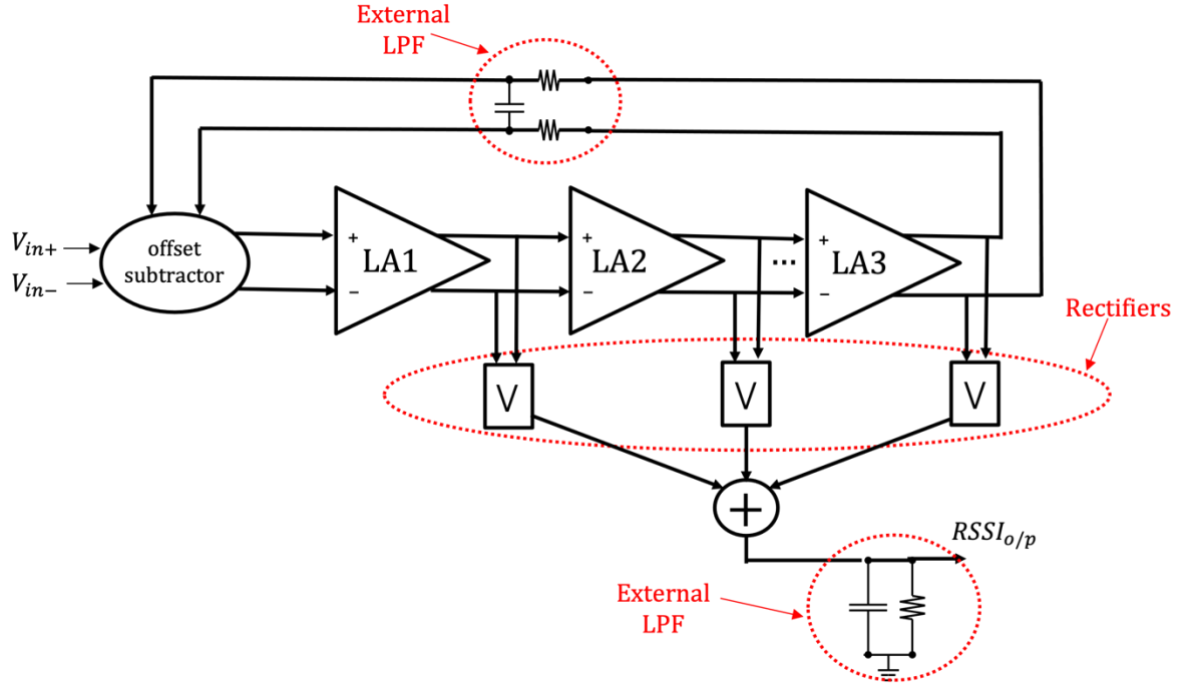


Figure 2. 2: RSSI conventional circuit architecture

Ideally, the RSSI output is a logarithmic function of the input signal's amplitude. However, in a successive detection architecture, such as Figure 2.2, the RSSI value is the sum of the output from all the branches. This is expressed in the equation below:

$$RSSI(V_I) = \sum_{i=0}^N x_i(V_I) \quad (1)$$

where N is the number of limiting amplifiers and $x_i(V_I)$ is the output of each branch. $x_i(V_I)$ is the DC level of the limiting amplifier and rectifier's output $A^i_{V_I}(t)$ which can be represented two ways based on its magnitude [5].

The case where it is less than the saturation voltage (V_s) is shown in Figure 2.3.a while the case where it is greater than the saturation voltage (V_s) is shown in Figure 2.3.b. It is reported in [5] that the RSSI error is the difference between the RSSI output of our desired architecture and the ideal logarithm function. Moreover, the RSSI dynamic range is the range of the input power which can be detected [6]. It is known to be the maximum input range where the RSSI error is less than 1 dB. In other words, the RSSI dynamic range is where the RSSI output is linear-in-dB.

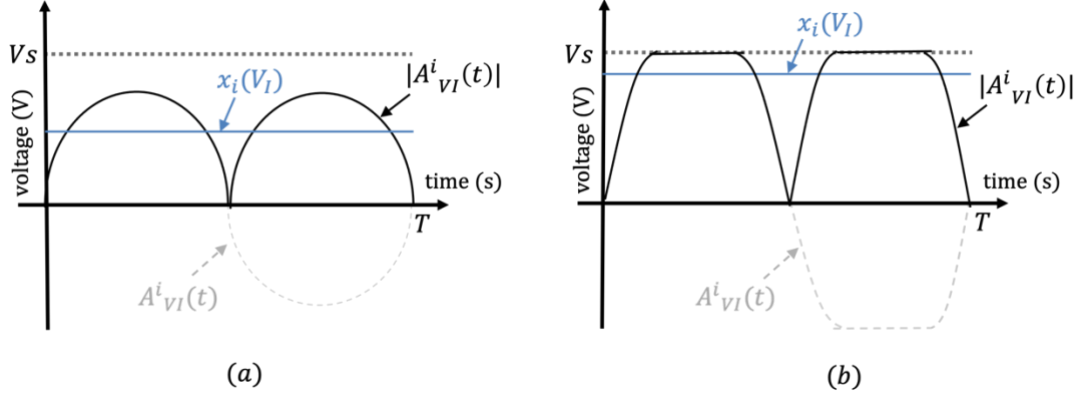


Figure 2. 3: Output voltage of each branch of the RSSI when it is (a) less than the saturation voltage (V_S) (b) greater than the saturation voltage (V_S)

Assuming all the limiting amplifiers have the same gain A , the RSSI dynamic range can usually be obtained using the equation below:

$$20\log_{10}(A^N) \quad (2)$$

Unlike dynamic range, which is the range of detectable input, detection sensitivity allows for the detection of changes in input power [6]. High detection sensitivity means it can detect small changes in input power. Both, wide dynamic range (DR) and high detection sensitivity (DS), are desirable for an efficient RSSI system depending on the application. However, there is a tradeoff between the two [7]. The equation for RSSI detection sensitivity is given by:

$$RSSI_{DS} = \frac{RSSI_{approx,max} - RSSI_{approx,min}}{RSSI_{DR,dB}} \quad (3)$$

It can be deduced from the above equation that if a low voltage supply is desired, yet still have sufficient dynamic range, the detection sensitivity will be reduced. It is important to measure our dynamic range. Nonetheless, the aim of this thesis is mainly to have high sensitivity level rather than a dynamic range because we want to detect very low inputs. However, when it comes to dynamic range, it will not be an issue since the aim is not for this RSSI to be greatly far from the target.

Successive detection RSSI architecture results in a piecewise linear curve rather than an ideal logarithmic curve.

The ideal logarithmic curve can be expressed as the following:

$$RSSI_{log}(V_I) = V_S \log_A \left(\frac{V_I}{V_S} \right) + NV_S \quad (4)$$

while the piecewise linear curve can be expressed as the following:

$$RSSI_{pl}(V_I) = \frac{A^{k+1}}{A-1} \left(V_I - \frac{V_S}{A^{k+1}} \right) + (N - k - 1)V_S \quad (5)$$

where N is the number of limiting amplifiers and k is between 1 and N.

Since an RSSI with successive detection architecture follows a piecewise curve, the maximum nonlinear error should be considered. The equation for maximum error is given in [8], where A is the gain per stage:

$$Error(dB) = \frac{10\{(-1+\sqrt{A}+A)\log A - (A-1)\log\left[A^{\left(\frac{3A-1}{2A-2}\right)}\right]\}}{A-1} \quad (6)$$

2.4. RSSI Topologies

The initial step in deciding the RSSI topologies that will be analyzed is knowing what type of amplifier works most effectively as an RSSI system. RSSI is also considered a power detector circuit. Using a bipolar junction transistor (BJT) for our power detector is not suitable for low-cost applications. Parameter variation significantly affects the behavior of the Schottky diode and BJT. Hence, the optimal solution would be to use a metal-oxide-semiconductor field effect transistor (MOSFET) logarithmic amplifier for a power detector because of its constant slope transfer curve corresponding to various decibel (dB) input power and wide dynamic range [9]. In [10] a simulated response of the AGC loop is shown to large amplitude steps for various detector types. It can be seen that in ‘Log’, the response is not slew-rate limited, and it is the fastest to recover from amplitude drops. The output of a logarithmic detector is proportional to the logarithm of the RF input voltage. The logarithmic amplifiers discussed and compared in this section are the most common topologies which are series linear limit, progressive-compression parallel-summation, parallel-amplification parallel-summation, and successive detection logarithmic amplifier (SDLA).

2.4.1. Series linear limit logarithmic amplifier

A series linear limit logarithmic amplifier is composed of cascaded dual gain stages, a high and a unity gain stage. This is illustrated in Figure 2.4. The high gain path has a smaller compression point than the unity gain path. Therefore, if the input has low power, it will be amplified, whereas if it has high power only the unity path will be

effective since the high gain path will be compressed [11].

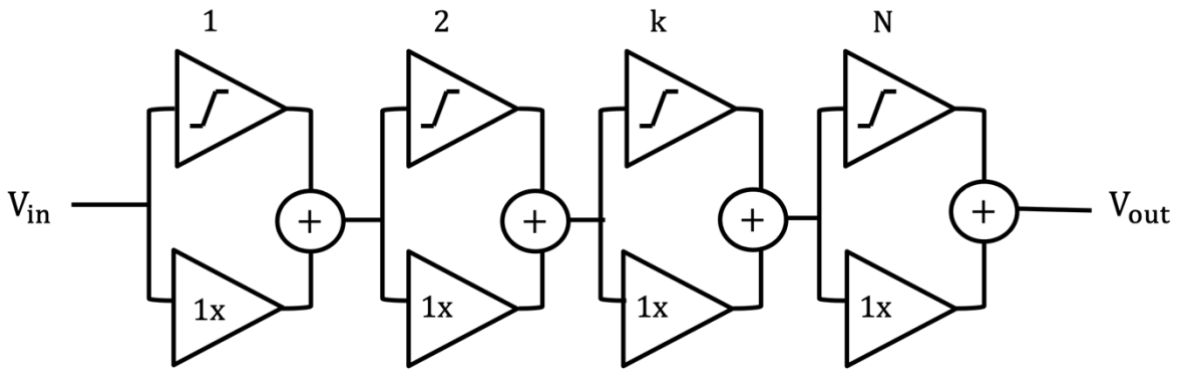


Figure 2. 4: Series linear limit logarithmic amplifier

A wide dynamic range can be obtained by either increasing the number of dual gain stages or increasing the gain of the dual gain stages [12]. However, increasing the gain also increases the logarithmic error which is not desired. Increasing the number of amplifier stages with smaller gain will result in a minimum logarithmic error.

2.4.2. Progressive-compression parallel-summation logarithmic amplifier

As in a series linear limit logarithmic amplifier, the gain stages in a Progressive-compression parallel-summation logarithmic amplifier are cascaded [12]. However, the output of the stages is summed in parallel to obtain the logarithmic amplifier output. The progressive-compression parallel-summation logarithmic amplifier is presented in Figure 2.5.

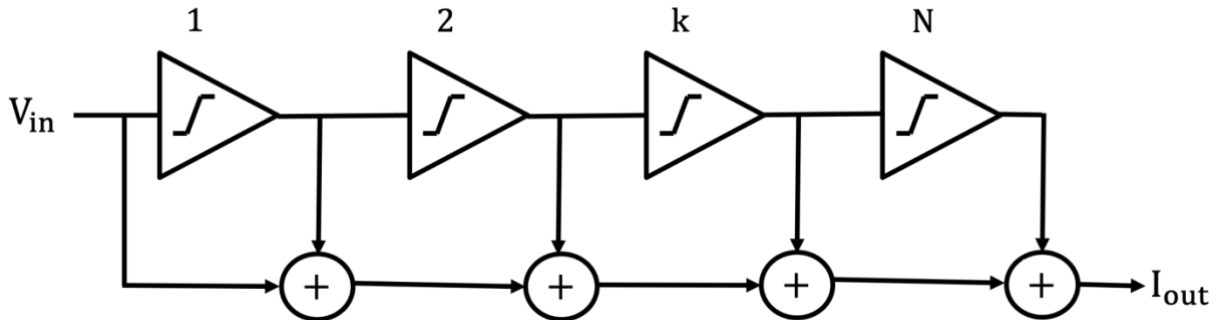


Figure 2. 5: Progressive-compression parallel-summation logarithmic amplifier

2.4.3. Parallel-amplification parallel-summation logarithmic amplifier

In a parallel-amplification parallel-summation logarithmic amplifier, shown in [12], the gain paths are independent of each other which is the reason why it is efficient for low dynamic range applications only [11]. Figure 2.6 represents a parallel-amplification parallel-summation logarithmic amplifier.

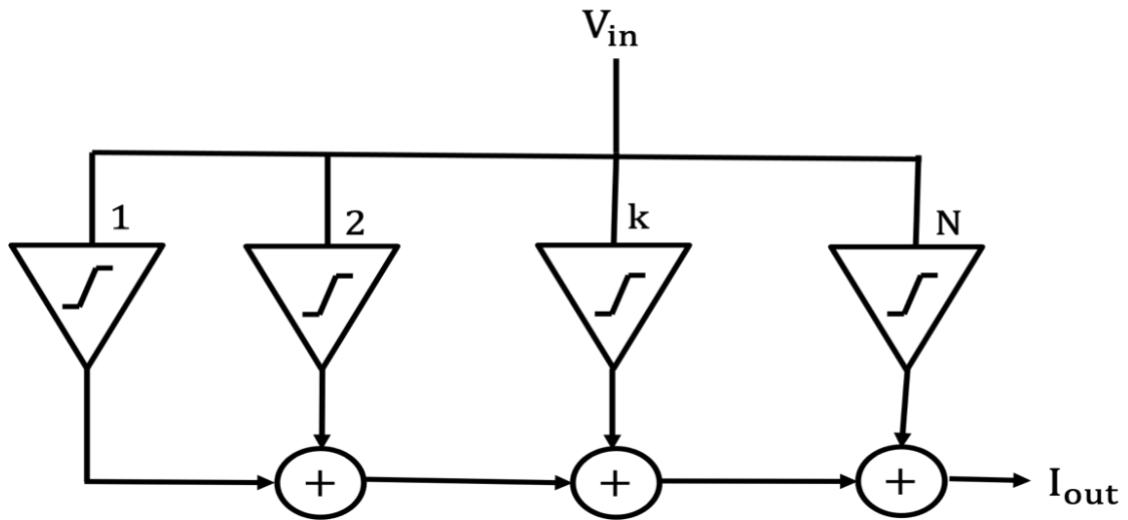


Figure 2. 6: Parallel-amplification parallel-summation logarithmic amplifier

Table 2.2 states the advantages and disadvantages of the previously mentioned logarithmic amplifiers.

Table 2. 2: Advantages and disadvantages of various logarithmic amplifiers

Type	Advantages	Disadvantages
Series linear limit	+Process variations affect each stage +Solution of phase equalization	-Because of loading: Limited BW
Progressive-compression parallel-summation	+High dynamic-range applications +No loading +high bandwidth	-Phase delay
Parallel-amplification parallel-summation	+Improved phase and group-delay matching	-Low dynamic-range applications

2.4.4. Successive detection logarithmic amplifier (SDLA)

The successive detection logarithmic amplifier shown in [12], illustrated in Figure 2.7, is very similar to the progressive-compression parallel-summation, except it includes a detector such as a half-wave rectifier or a full-wave rectifier.

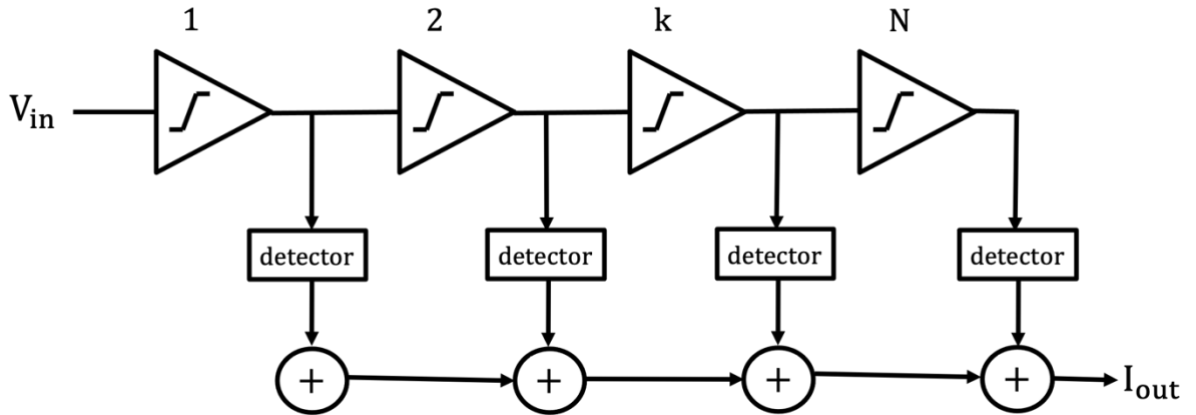


Figure 2. 7: Successive detection logarithmic amplifier (SDLA)

2.5. RSSI for Localization

After the received power levels within the desired dynamic range are detected by the RSSI system, it is time to discuss RSSI for localization. The distance between the drone and the WPT transmitter can be obtained using the equation below:

$$RSSI = -10n\log_{10}(d) + P1[dB] \quad (7)$$

where RSSI is the value obtained from our RSSI system, $P1$ is the power received at one meter from the WPT transmitter, n is the path loss of the propagation, and d is the distance between the transmitter and the receiver [13]. Using RSSI output (mV) versus Input power (dBm) plot in logarithmic scale as shown in reference [14], the RSSI output power, as well as the input power, can be identified which can be used later for distance estimation. Path loss factor can be due to various reasons such as free-space loss, refraction, diffraction, reflection, and absorption. In this section, the drone is considered to be the transmitter while the WPT transmitter is considered to be the receiver in order to localize it, hence, an RSSI receiver system must be placed in the WPT transmitter. For this thesis' scenario, where the drones are expected to be used for a smart farm, using this method for localization will be very practical, as it is cost-effective and the pathloss effect would not be a huge issue since smart farms are not usually located in dense locations with a lot of infrastructure.

To know the location of the WPT transmitter, a method called 'Trilateration' is used where spheres are drawn around each transmitter, drone in this thesis' application, representing its coverage area, and the area at which all spheres intersect will be the location of the receiver, which is the WPT transmitter as shown in Figure 2.8.

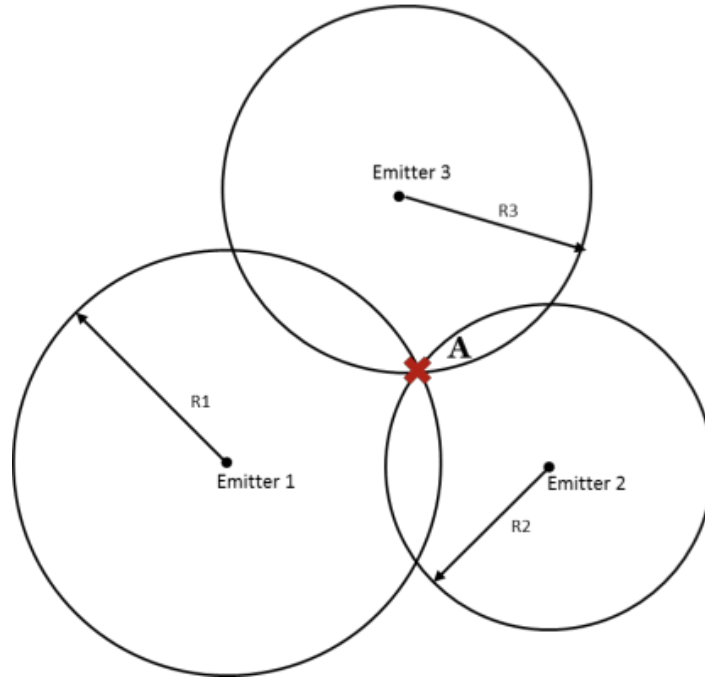


Figure 2. 8: Trilateration for the localization of the WPT transmitter

The minimum number of drones needed for trilateration is 3 drones. However, the intersection of 3 spheres could be 2 points. Therefore, it is better to have a 4th drone to solve this ambiguity by eliminating one of the two possible positions. Nonetheless, the more drones used, the more accurate the positioning coordinates are which aligns with the application targeted in this thesis since significantly more than 3 drones will be used for various functions in a smart farm in addition to localization.

Although obtaining distance estimation for wireless sensor networks (WSN) using RSSI is a very efficient solution cost-wise, however, because RF propagation is almost always affected by obstacles whether man-made or natural, the distance estimates end up with large errors. Thus, in [15] outlier detection methods on three different localization schemes are proposed to reduce the error resulting in location estimation using RSSI. The proposed detection method is a centroid-based outlier detection scheme that applies a clustering mechanism on the candidate location estimates to identify the location of the highest agreement. A clustering grid is shown in Figure 9 of reference [15] which uses centroid-based outlier detection where the red dots represent the trilateration results, the blue square identifies the grid with the highest number of mapped location estimates, and the centroid of the blue square would be the final estimated location of the target.

2.6. Related Work

In [7], programmable reference bias current controls within the full-wave rectification circuit to allow for the tradeoff between the dynamic range and detection sensitivity of the RSSI system are proposed. In [16], a DR scalable RSSI is proposed which provides 2 modes: high detection sensitivity and wide dynamic range depending on the type of detection desired. However, in both papers [7] and [16], high detection sensitivity and wide dynamic range cannot be achieved simultaneously as illustrated in Figure 1(b) in [6]. A piecewise RSSI to achieve a wide dynamic range and high detection sensitivity simultaneously is proposed in reference [6]. That was accomplished by dividing the dynamic range, from -80 dBm to 0 dBm, into 4 sub-ranges. The full-wave rectifier in this case is a function of the reference bias current (I_{ref}) and input signal. I_{ref} controls the dynamic range of each subrange, and the rectifier's input depends on the input signal strength and limiting amplifiers' gain. Turning some of the limiting amplifiers on and off allows the transfer curve to be shifted among the sub-ranges. By applying this technique, the dynamic range and the detection sensitivity are both enhanced as shown in the transfer curve represented in Figure 1(c) in [6].

Moreover, in [6] and [7], a two-path Inphase/Quadrature configuration to reduce the output voltage glitch is proposed. Equation (8) represents the output current using a traditional single-path RSSI, and equation (9) represents the output current using a two-path I/Q RSSI. It can be concluded that using the I/Q configuration, the 2nd-order harmonic component can be canceled.

$$I_{total} = \sin^2(\omega t) + \cos^2(\omega t) = 1 \quad (8)$$

$$I_{total} = \sin^2(\omega t) = \frac{1}{2} - \frac{1}{2}\cos(2\omega t) \quad (9)$$

Various RSSI system simulated and measured results from previous work will be discussed later at the end of Chapter 4 to compare with the simulated results from the proposed RSSI of this thesis.

Chapter 3. Proposed Work

This thesis proposes a highly effective RSSI with linear-in-dB behavior designed for wireless power transfer receiver systems. The RSSI will be implemented using TSMC 65nm RFCMOS process. To ensure the proposed RSSI achieves desired signal detection and coverage, it is designed such that it has high detection sensitivity and low power consumption. The architecture used for the proposed RSSI follows successive detection logarithmic amplifier (SDLA) topology as shown in Figure 2.7 due to its logarithmic behavior that leads to better detection as discussed in Chapter 2. All the limiting amplifiers in an SDLA architecture should be identical to minimize logarithmic error. This chapter will discuss the proposed design specifications and the chosen design for the RSSI's limiting amplifier and rectifier.

3.1. Proposed RSSI Specifications

Ensuring the system will be able to detect the minimum power input based on the power transmitted from the WPT transmitter is the first step in deciding on the proposed RSSI system specifications. What is known about the WPT transmitter is that the transmitted power is 20 dBm which is equivalent to 100mW and that it can reach up to 6 to 10 meters from the transmitter. This is an acceptable and safe ISM transmitted power according to Telecommunications and Digital Regulatory Authority in the United Arab Emirates [17]. Since our distance is relatively small, it is fair to use the free space path loss model.

$$\begin{aligned} FSPL(dB) &= 10 \log_{10} \left(\left(\frac{4\pi df}{c} \right)^2 \right) \\ &= 20 \log_{10} \left(\frac{4\pi df}{c} \right) \\ &= 20 \log_{10}(d) + 20 \log_{10}(f) + 20 \log_{10} \left(\frac{4\pi}{c} \right) \\ &= 20 \log_{10}(d) + 20 \log_{10}(f) - 147.55 \end{aligned} \quad (10)$$

The above equation is applied for isotropic antennas. Since the transmitting and receiving antennas expected for this work will be directional and not isotropic, the gains of the antennas should be introduced as indicated in the Friis transmission equation below [18]:

$$FSPL = 20 \log_{10}(d) + 20 \log_{10}(f) + 20 \log_{10} \left(\frac{4\pi}{c} \right) - G_t - G_r \quad (11)$$

given:

$f = 5.8 \text{ GHz}$ (An ISM band according to ITU 5.150 [19])

$d = 6 \text{ to } 10 \text{ m}$ from the transmitter

Transmitted Power (P_t) = 20 dBm

$$P_R = P_t - P_L(d) \quad (12)$$

Equation (12) expresses the received power at the RSSI's front end where P_R is the received power, P_t is the transmitted power, and P_L is the free space path loss.

The received power is usually presented in terms of dBm. The below equation is used for the conversion between dB to dBm:

$$\text{dBm} = \text{dB} + 30 \quad (13)$$

Assuming transmitter antenna gain (G_t) and receiver antenna gain (G_r) = 10 dB

$$P_L = 20 \log_{10}(d) + 20 \log_{10}(f) - 147.55 - 10 - 10$$

$$\text{for } d_1 = 6 \text{ m} : P_L = 43.28 \text{ dB} = 73.28 \text{ dBm}$$

$$\text{for } d_2 = 10 \text{ m} : P_L = 47.7 \text{ dB} = 77.7 \text{ dBm}$$

using equation (12):

$$A_1 = 20 - 73.28 = -53.28 \text{ dBm}$$

$$A_2 = 20 - 77.7 = -57.7 \text{ dBm}$$

The RSSI is expected to be placed on a flying drone which will detect the signal from the wireless power transfer transmitter. The WPT transmitter is designed to emit a signal of 20 dBm power at 5.8 GHz. Assuming the transmitter and antenna gains are equal to 10 dB, it can be deduced using equations (11) and (12) that the power received by the RSSI system is around -57 dBm at 10m from the transmitter. The power specification is then converted to voltage assuming input impedance equals 50 ohms, The received voltage would be 0.41mV at 10m away from the transmitter.

The proposed RSSI desired specifications are shown in Table 3.1. Since the received voltage is around 0.41mV, the sensitivity level specification becomes 0.3 mV with a 0.11mV safety margin. With regards to the frequency specification, 5.8 GHz is chosen as it is an available ISM band. An advantage of high frequencies is to allow for smaller size components on the receiver side such as filters and antenna.

Table 3. 1: RSSI desired specifications

	Value	Unit
Supply Voltage	1	V
Frequency	5.8	GHz
Power	< 30	mW
Sensitivity level	< 0.3	mV
Dynamic Range	40	dB
Technology	65	Nm

3.2. Proposed RSSI Design

This thesis focuses on the limiting cell and full-wave rectifier design. Different designs are compared in this section as discussed in previous work and justify the chosen option. MOSFET transistors are used for the RSSI of this thesis due to their lower power consumption as they are voltage-controlled devices with no gate current, contrary to BJT. MOSFETs also have much higher input impedance, less noise, and smaller size.

3.2.1. Limiting amplifier design

A traditional limiting amplifier design which is shown in Figure 3.1 has the advantage of as easily adjusting the gain, expressed in equation (14), since it only depends on the input transistor size and load transistor size [20]. However, the limiting amplifier design chosen is the one shown in Figure 3.2 due to the following reason: In the CMOS process, the NMOS load transistors suffer from the body effect which impacts the gain. The body effect is an important factor that needs to be taken into consideration when designing any circuit. It refers to the voltage difference between the transistor source and body resulting in a change in the transistor threshold voltage [21]. Current mirrors in Figure 3.2 are used to eliminate that body effect. This design is also made to eliminate the influence of process variation on the gain [22]. Moreover, the output is taken differentially due to the many advantages associated with a fully differential design. Some of those benefits include a high common mode rejection ratio, a high power supply rejection ratio, and a wide dynamic range. Common-mode rejection ratio (CMRR) refers to the immunity of a circuit against any undesirable common-mode signals that might appear at the input, while power-supply rejection ratio (PSRR) indicates the immunity of a circuit against supply noise or other disturbances on the supply rail that can propagate to the amplifier's output [23].

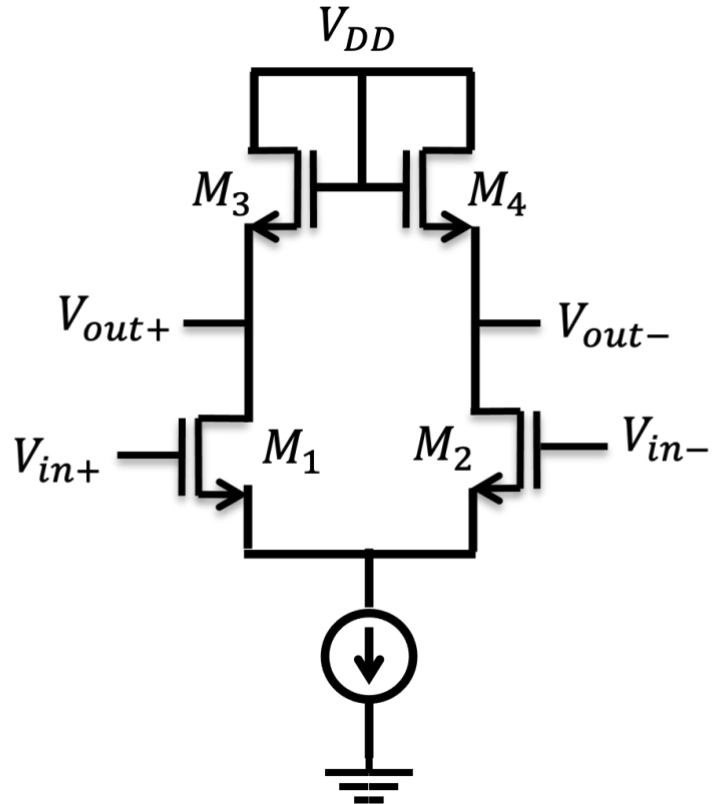


Figure 3. 1: Traditional limiting amplifier

$$A = \frac{g_{m1}}{g_{m3}} = \frac{\sqrt{(W/L)_1}}{\sqrt{(W/L)_3}} \quad (14)$$

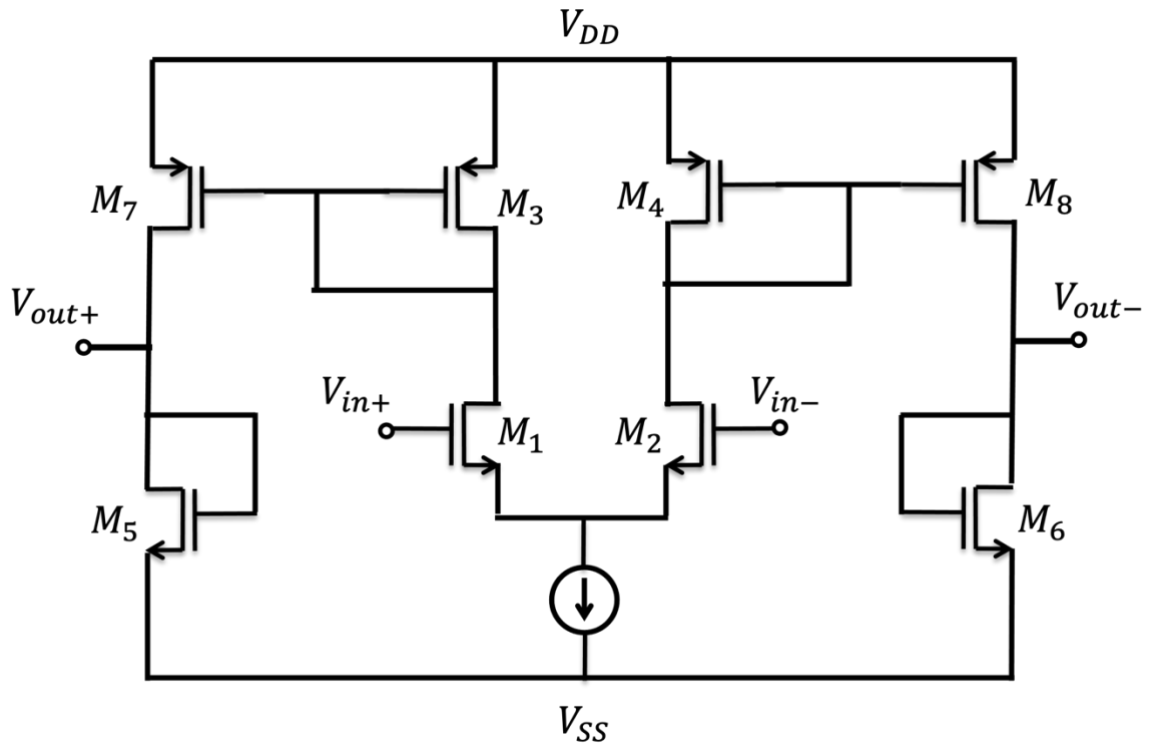


Figure 3. 2: Limiting cell circuit schematic

3.2.2. Full-wave rectifier design

Full-wave rectifiers are needed in any RSSI system as they convert AC to DC. DC RSSI output is more convenient to approximate the power level since it is a fixed amplitude without the need to worry about phase contribution, which makes it easier to be digitized. Full-wave rectifiers (FWR) are also desired since they act as voltage-to-current converters, allowing the output of all the stages to be summed without the need for adders. Although a rectifier can be realized using diodes, they are limited by their threshold voltage. Since diodes will undoubtedly be a bad choice for the RSSI because of their large threshold voltage which will make it difficult to operate cascaded stages, hence, precision rectifiers that are capable of rectifying voltages with very small magnitudes are required.

In [24], the circuit design of a precision full-wave rectifier is presented as shown in Figure 3.3. The precision full-wave rectifier with current inputs will require the use of voltage to current converters after each limiting amplifier and then to FWR which would consume more power than needed. Thus, this FWR design is not suitable for the proposed application of this thesis. For lower power consumption, it makes more sense to use an FWR that would also act as a voltage-to-current converter since the proposed limiting cell output is voltage rather than current. Therefore, the full-wave rectifier design chosen for the proposed RSSI system is shown in Figure 3.4. In this design, the size of one of the differential pairs is k times larger than the other. If the input voltage is small, the larger transistors will contribute to most of the current. Hence, its corresponding current mirror will have a larger current flow than that which is connected to the smaller-size transistors. When input starts to increase, the smaller-size transistors start to accept current flow from the current mirror corresponding to the smaller transistors. Therefore, the current mirror for the larger transistors decreases [20]. What makes this rectifier design precisely unique is that it accepts extremely small inputs. Equation (15) represents the output current equation.

Chapter 4. Results and Discussion

In this chapter, simulation results of the transistor level circuit of the proposed RSSI using cadence virtuoso with TSMC 65 nm library are presented. The main RSSI components which are discussed in this chapter are the limiting cell and full-wave rectifier.

4.1. Limiting Cell

The limiting cell used in the proposed RSSI is as shown in Figure 3.2. In this section, first, the size of the load transistors, M5 and M6, is varied to study its effect on the output. The behavior of cascaded limiting stages with diodes from a general perspective is then analyzed. This section also discusses the simulation results regarding frequency and input amplitude sensitivity. Lastly, details on the component sizes and values of the proposed limiting cell are presented in addition to each component's functionality.

4.1.1. Effect of load transistors size

Output voltage (v_{out}) versus input voltage (v_{in}) behavior of a single limiting cell for different width sizes of load transistors, M5 and M6, is represented in Figure 4.1, using the parametric analysis tool in cadence virtuoso.

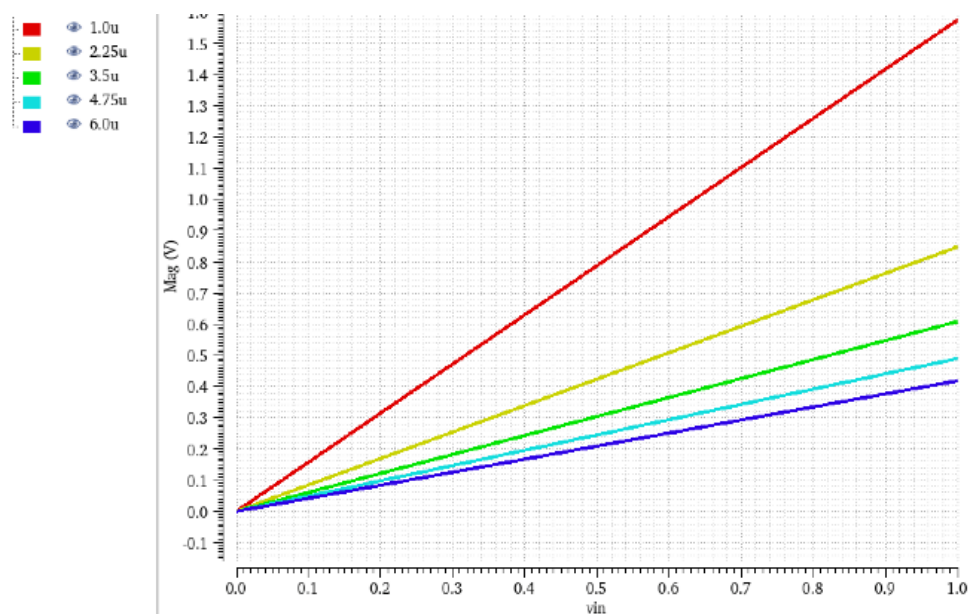


Figure 4. 1: V_{out} vs. v_{in} of a limiting cell for different load transistors widths

The width is varied from 1u to 6u with the number of fingers in each being equal to 10. This means the total width of the nmos load transistors is varied from 10u to 60u. It can be noticed that the smaller the width of the load transistor, the higher the gain.

4.1.2. Limiting cascaded stages behavior

Before setting the limiting cell gain to a desired value based on the proposed specifications, the behavior of cascaded limiting stages with diodes from a general perspective needs to be studied. Figure 4.2 represents the output of four limiting cells being cascaded when the input is 50mV. It can be noticed that from the output of the first stage (out1) to the last cascaded stage (out4), the output is increasing which means the limiting cell gain is positive, making it act as an amplifier.

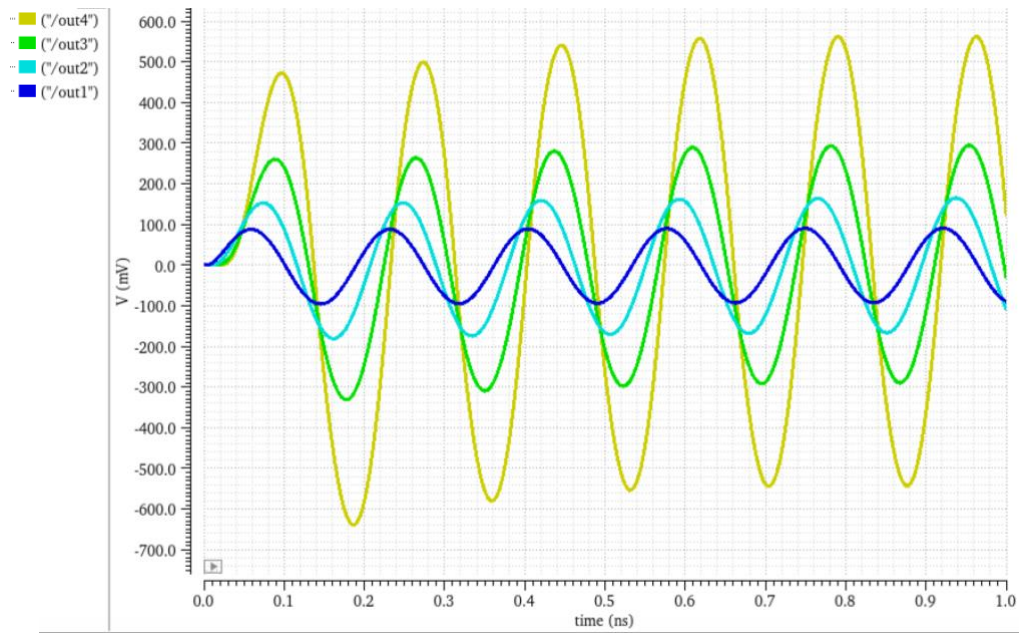


Figure 4. 2: Output of cascaded limiting stages

In order to observe the v_{out} vs. v_{in} behavior in cadence, the transient analysis must be used. For cadence virtuoso to allow us to do that, the “ymax” function should be used for the output and parametric analysis to sweep the input as shown in Figure 4.3. Figure 4.4 shows the half-wave rectified output after each stage. It can be observed that the outputs are significantly small, in nanovolts. That is because the 4th cascaded limiting stage output seems to be just above the diode threshold. The second row of Figure 4.4 (a-d) is the v_{out} vs. v_{in} behavior of each stage in linear scale, while the third row is the v_{out} vs. v_{in} behavior in logarithmic scale. By cascading more stages, the output becomes closer to a piece-wise logarithmic output as discussed in the literature review, and the linear-in-dB shown in the logarithmic scale plot is increasing which means a larger dynamic range, hence, better detection.

Expression `ymin((VT("/Vout+") - VT("/Vout-")))` From Design

Calculator Open Get Expression Close

Will be Plotted/Evaluated

Parametric Analysis - spectre(0): Thesis_RSSI Limiting_amp2 schematic

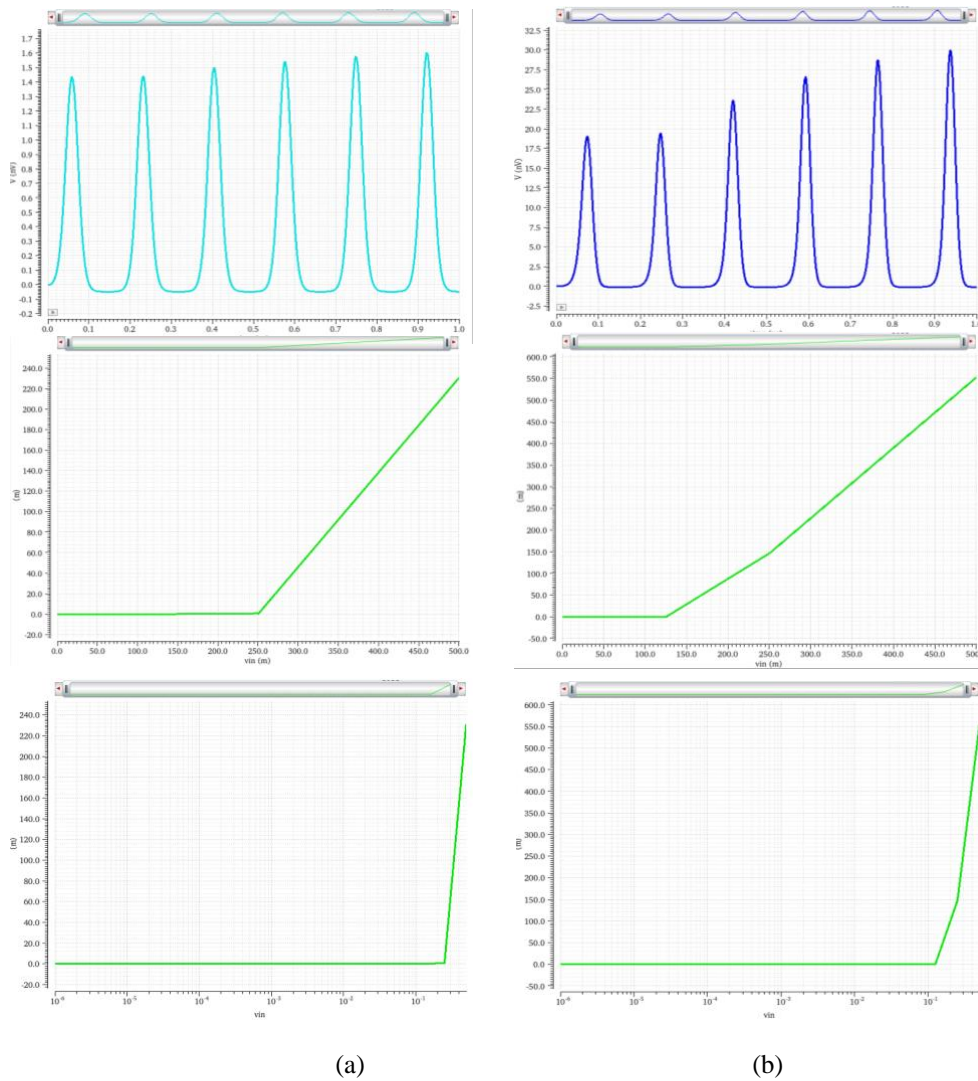
File Analysis Help

Parametric Simulation Completed.

Run Mode: Sweeps & Ranges

Variable	Value	Sweep?	Range Type	From	To	Step Mode	Total Steps	Inclusion List	Exclusion List
vin	100m	<input checked="" type="checkbox"/>	From/To	1u	3	Auto	20		

Figure 4. 3: Function “ymin” for the output and parametric analysis to sweep input



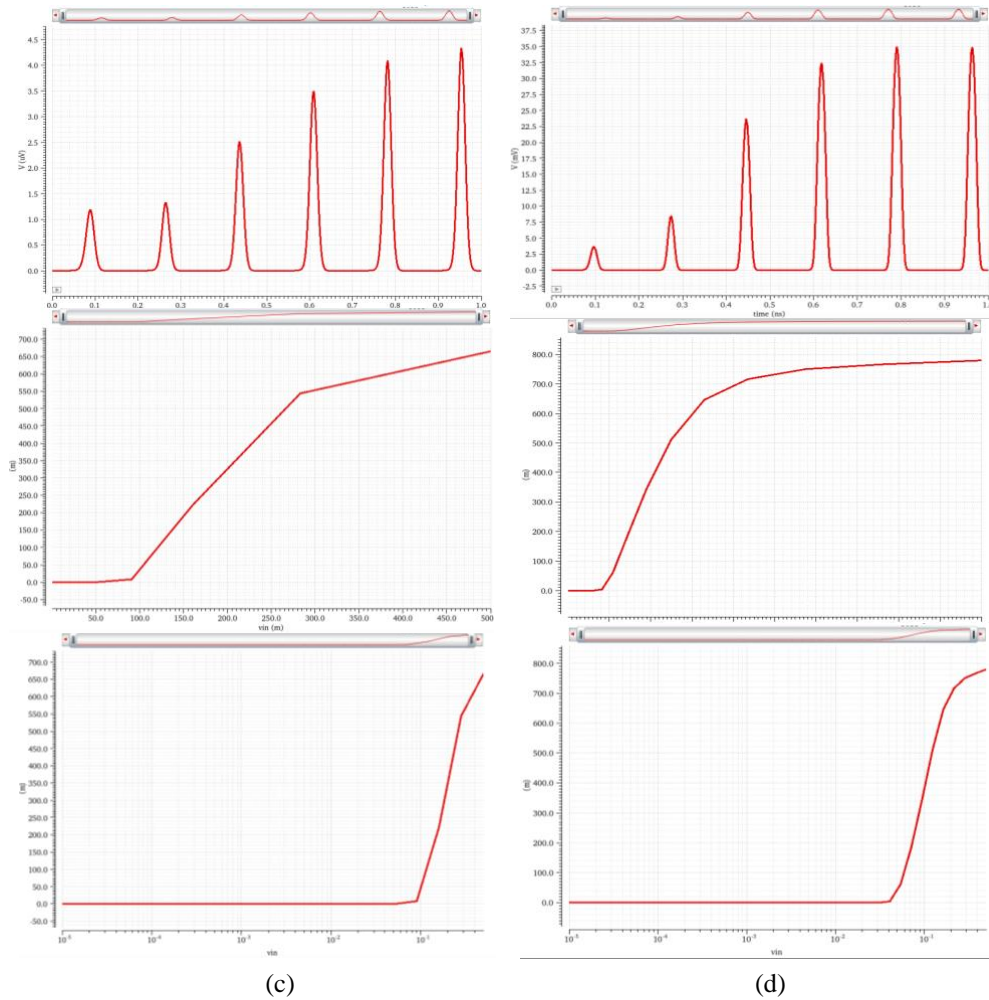


Figure 4. 4: Output after (a) 1 stage (b) 2 stages (c) 3 stages (d) 4 stages

The frequency response of a single-stage limiting cell is shown in Figure 4.5. The sizing of the transistors is adjusted to have the limiting amplifier set at around 0.3 gain at the target frequency of 5.8 GHz. The input signal must be attenuated for our chosen FWR design since it is made to function only for very small signals as studied in the previous chapter. This will be discussed further in section 4.2 where the FWR simulation results are presented. Now that the gain of the proposed limiting cell is set to 0.3, the maximum error can be calculated using equation (6). By taking the absolute value of the result, we get a 0.4 dB error.

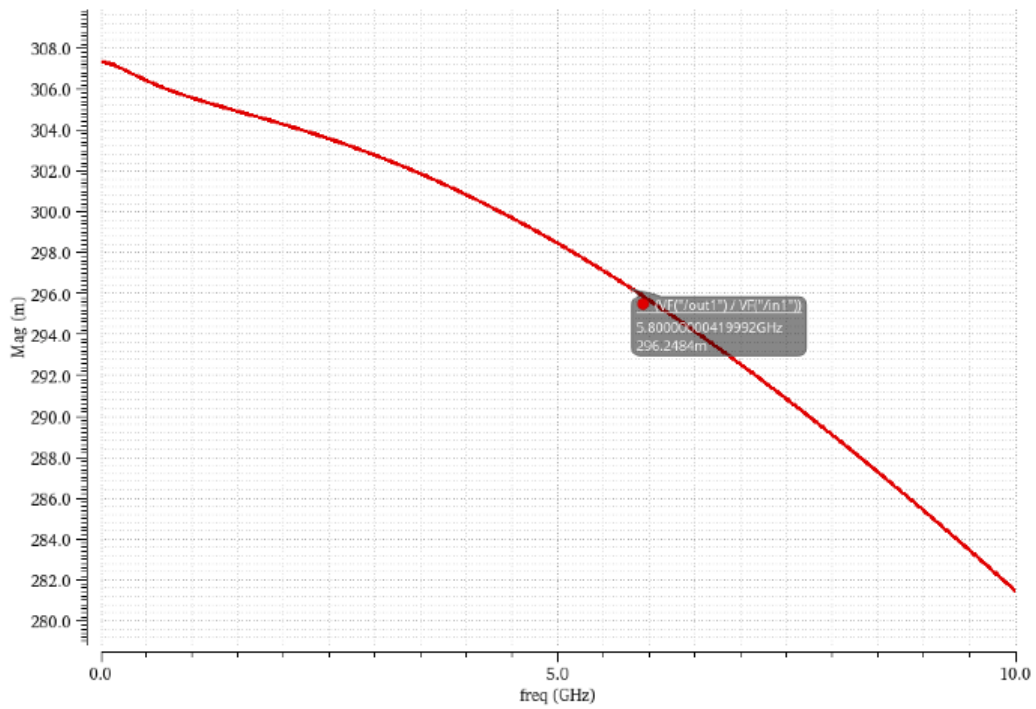
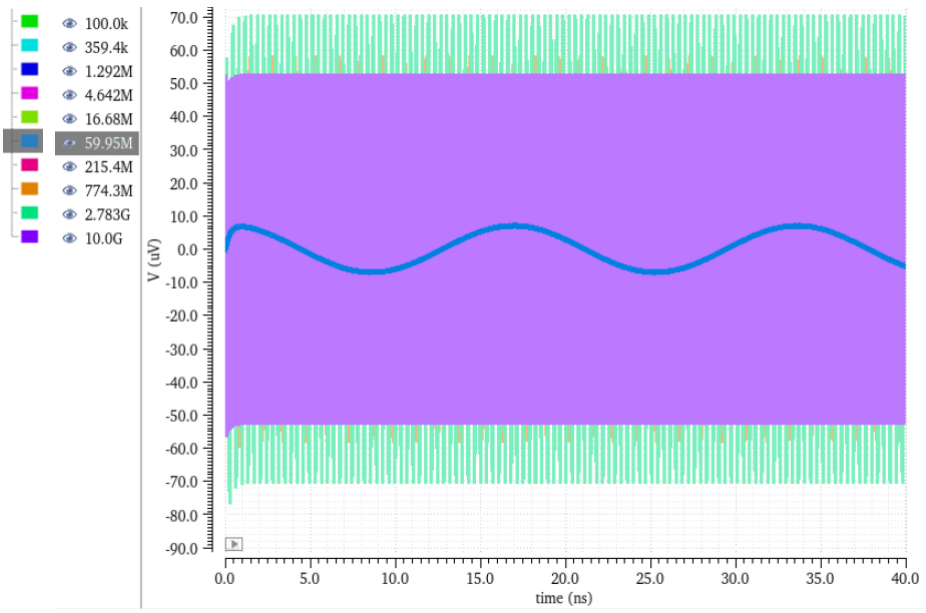


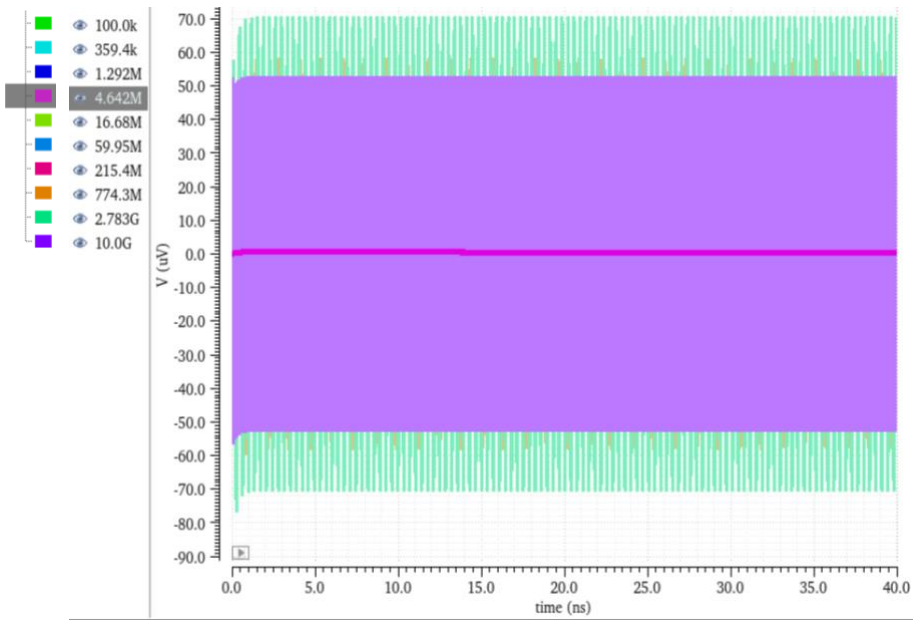
Figure 4. 5: Frequency response of a single-stage limiting cell

4.1.3. Frequency sensitivity

Although the desired gain has been adjusted for the targeted 5.8 GHz signal, it is still important to see the limiting cell's behavior with various frequencies in case the system is used for other applications. In Figure 4.6.a and Figure 4.6.b, the input frequency of the 0.41mV signal is varied, and then the behavior of the limiting cell output is observed to find out the frequency sensitivity level. Because the frequency and amplitude of a signal have an inverse relationship, it is shown in Figure 4.7 that as input frequency increases, the output amplitude decreases. Therefore, at 80 GHz frequency, the output amplitude is significantly smaller. Thus, this means the proposed RSSI system works for applications with frequencies 50 MHz to 80 GHz. Due to that, the proposed RSSI circuit is suitable for 5G and 6G applications.



(a)



(b)

Figure 4. 6: (a) Limiting cell output with minimum input frequency (b) Limiting cell output with an input below minimum frequency

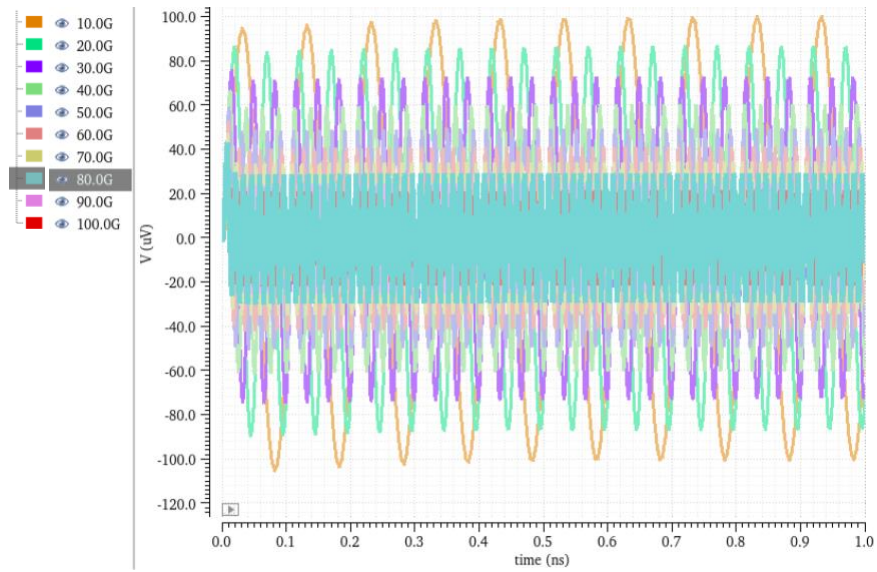


Figure 4. 7: Limiting cell output with maximum acceptable input frequency

4.1.4. Maximum acceptable input

Figure 4.8 shows that limiting cell output is being clipped starting from around 700mV input which will not be an issue since the signal received from the WPT that's aim is to charge the receiver drones can reach a maximum of 0.679mV at the receiver's front end.

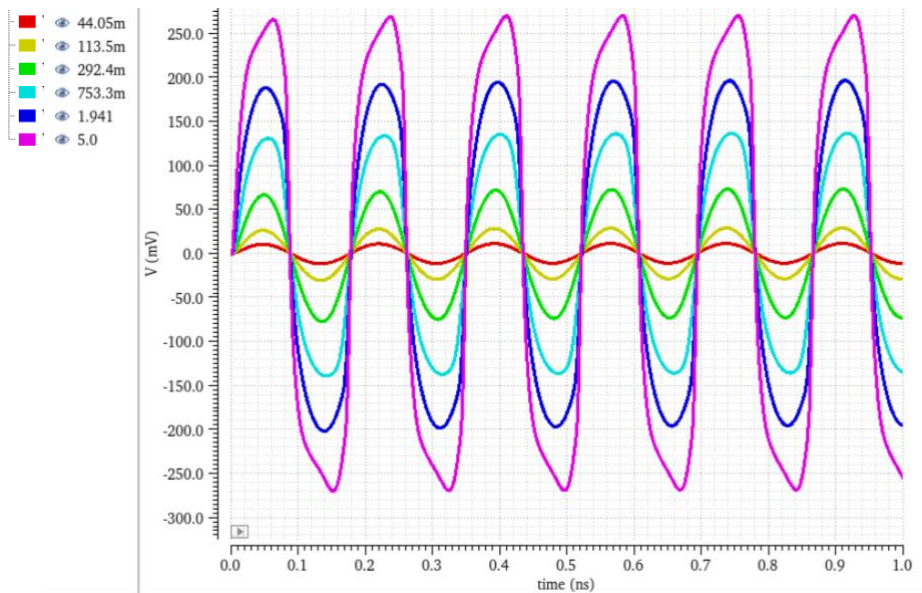


Figure 4. 8: Limiting cell output given various input levels

4.1.5. Limiting cell components parameters

Table 4.1 details the component sizes and values of the proposed limiting cell in cadence virtuoso whereas Table 4.2 highlights the proposed limiting cell's components functions.

Table 4. 1: Proposed limiting cell components sizes and values

Component	Width	Length	Fingers
M3,M4,M7,M8	2 um	60 nm	16
M1,M2	3 um	60 nm	9
M5,M6	6 um	60 nm	20
Current tail NMOS	2 um	60 nm	16

Table 4. 2: Proposed limiting cell components functionality

Component	Function
M3,M4,M7,M8	Current Mirrors
M1,M2	Attenuators
M5,M6	Loads

The expected dynamic range can be determined by following the steps below:

$$A=0.3$$

$$N=4$$

$$0.3^4 = 8.1\text{m}$$

$$\text{Dynamic Range} = 20 \cdot \log(8.1\text{m}) = -40 \text{ dB} = 40 \text{ dB}$$

where A is the gain of the limiting cell and N is the number of limiting cells to be cascaded.

4.2. Full-Wave Rectifier

The full-wave rectifier simulated for the proposed RSSI is shown in Figure 3.4. Figures 4.9 and 4.10 show the output of the limiting cell and full-wave rectifier respectively before adjusting the limiting cell to act as an attenuator. The input is the targeted WPT signal input at 6 meters from the transmitter which is 0.679mV. As observed, the proposed rectifier does not rectify large input signals, and it seems that it considers the input too large.

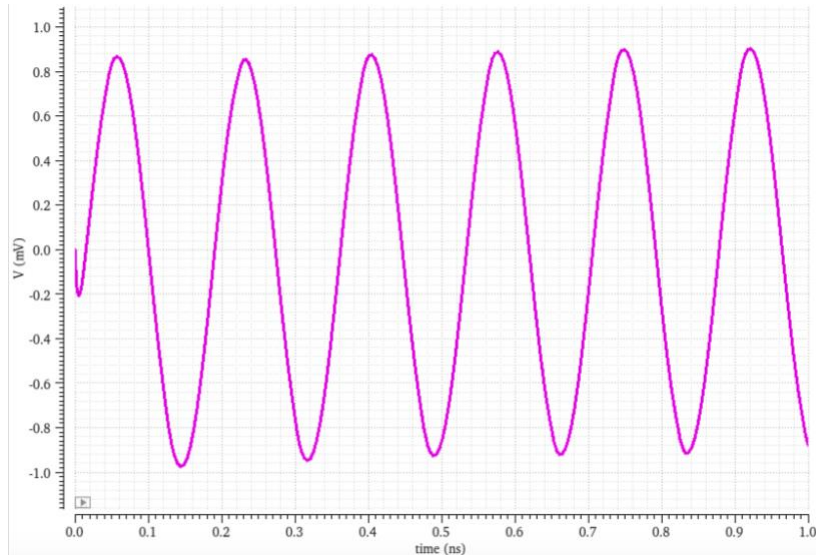


Figure 4. 9: Limiting cell output before adjusting limiting cell gain

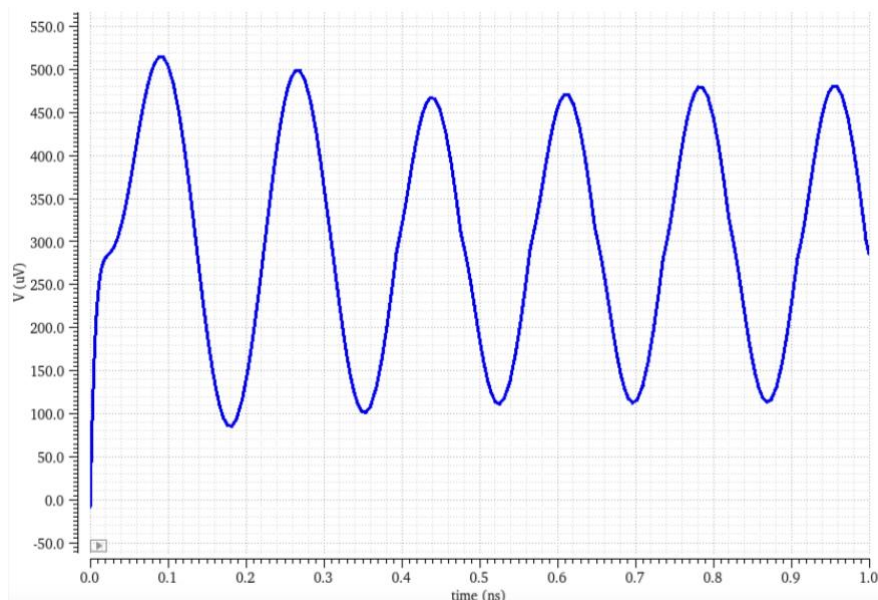


Figure 4. 10: Full-wave rectifier output before adjusting limiting cell gain

The output of all the full-wave rectifiers of the cascaded limiting stages after adjusting the limiting cells will be part of the RSSI output results section.

4.2.1. FWR sensitivity level

In this section, the sensitivity level of the full-wave rectifier (FWR) of the proposed RSSI is measured. The input to the FWR is connected to a separate input at first to study the behavior of the output. Figure 4.11 shows the current of one of the rectifier branches given different input levels. It can be noticed that as input increases, the current is showing AC behavior. Therefore, the input of the FWR must not exceed 100 uV. This

is the reason the gain is set to 0.3 as mentioned previously such that the expected input will be reduced as it propagates through the stages.

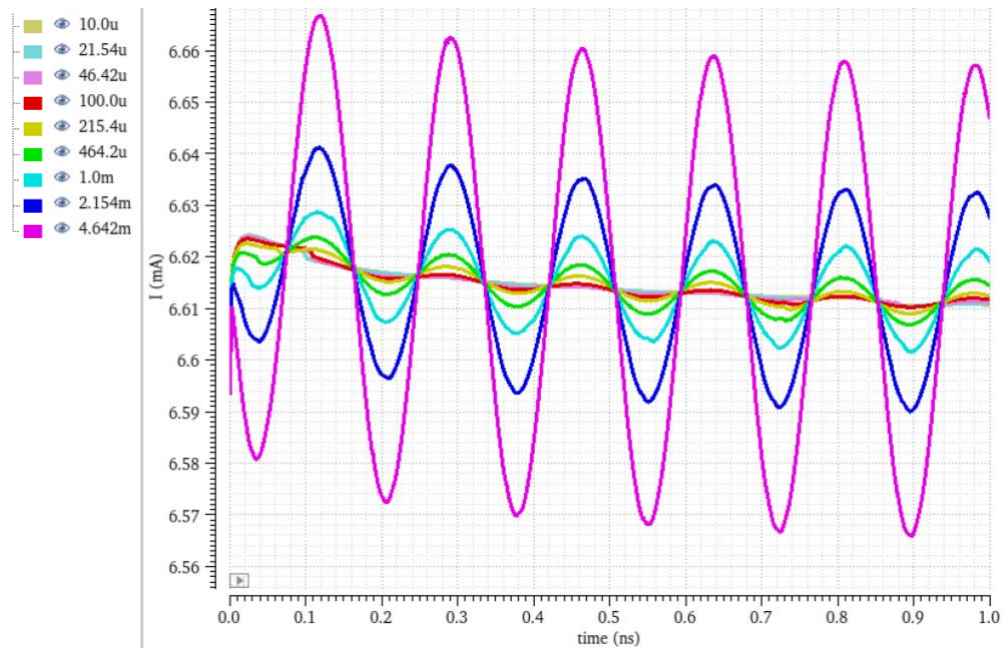


Figure 4. 11: Rectifier branch current given different input levels

4.2.2. FWR components parameters

Table 4.3 details the component sizes and values of the proposed FWR in cadence virtuoso whereas Table 4.4 highlights the proposed FWR's components functions.

Table 4. 3: Proposed FWR components sizes and values

Component	Width	Length	Fingers
M5,M7	2 um	60 nm	16
M6,M8	2 um	60 nm	16
M1,M4	2 um	60 nm	16
M2,M3	6 um	60 nm	20
Current tail NMOS 1	2 um	60 nm	16
Current tail NMOS 2	2 um	60 nm	16

Table 4. 4: Proposed FWR components functionality

Component	Function
M5,M7	Current Mirrors controlled by smaller size rectifier transistors
M6,M8	Current Mirrors controlled by larger size rectifier transistors
M1,M4	smaller size rectifier transistors
M2,M3	larger size rectifier transistors

4.3. RSSI Circuit

The proposed RSSI circuit schematic in cadence virtuoso is shown in Figure 4.12. It consists of cascaded limiting amplifiers where the differential output of each stage is taken as input to the full-wave rectifiers, and a low pass filter at the end to remove the ripples at the output as it is used to eliminate the AC contribution in the output.

4.3.1. RSSI limiting stages output

Figure 4.13 represents the limiting stages cascaded outputs where (a) is after the first stage till (d) which is the cascaded 4 stages limiting output when input is equal to 0.41 mV. None of the limiting stages' outputs appears to exceed 100 uV. Hence, it is safe to proceed with the next step which is to observe the RSSI's output.

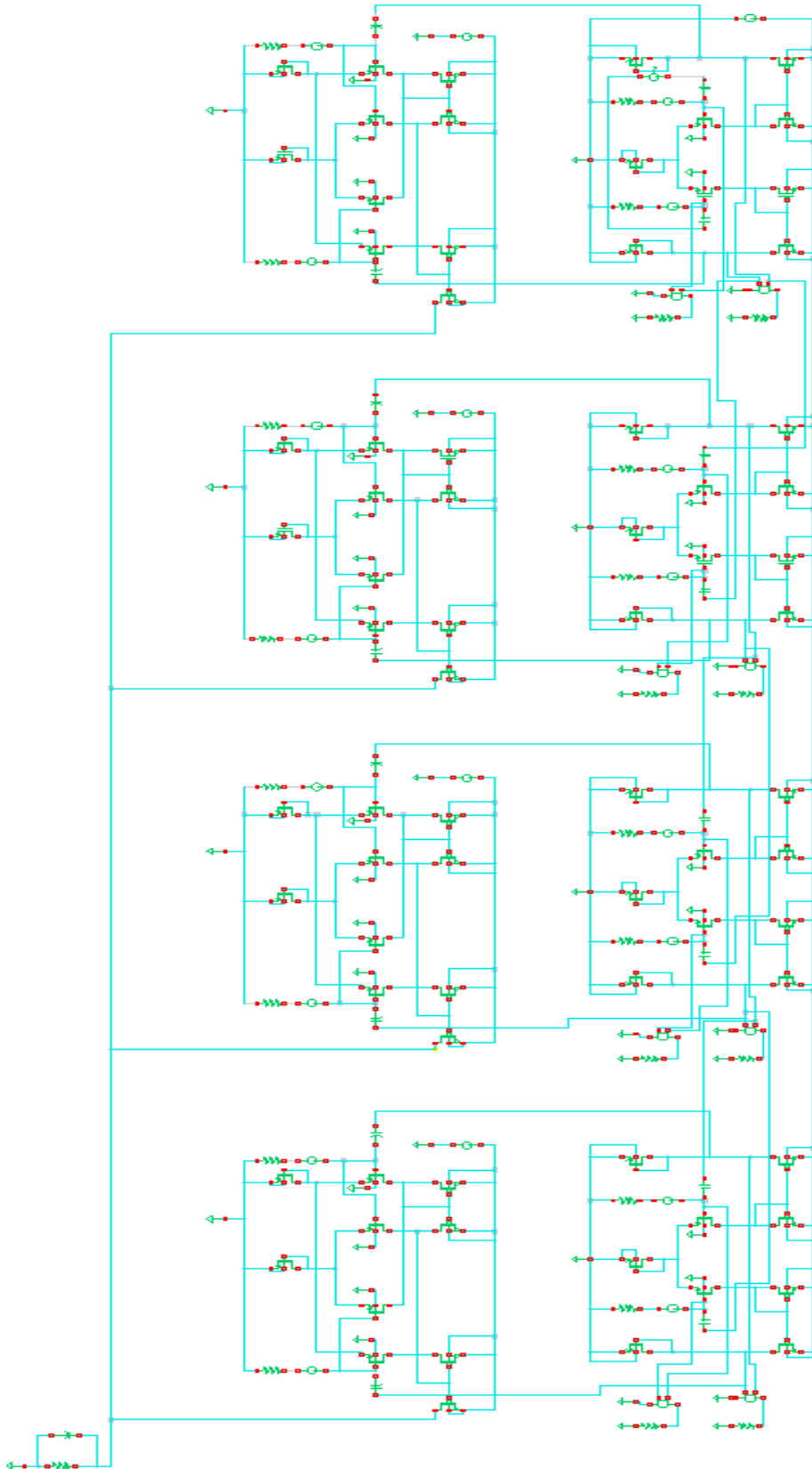


Figure 4. 12: RSSI circuit schematic on cadence virtuoso

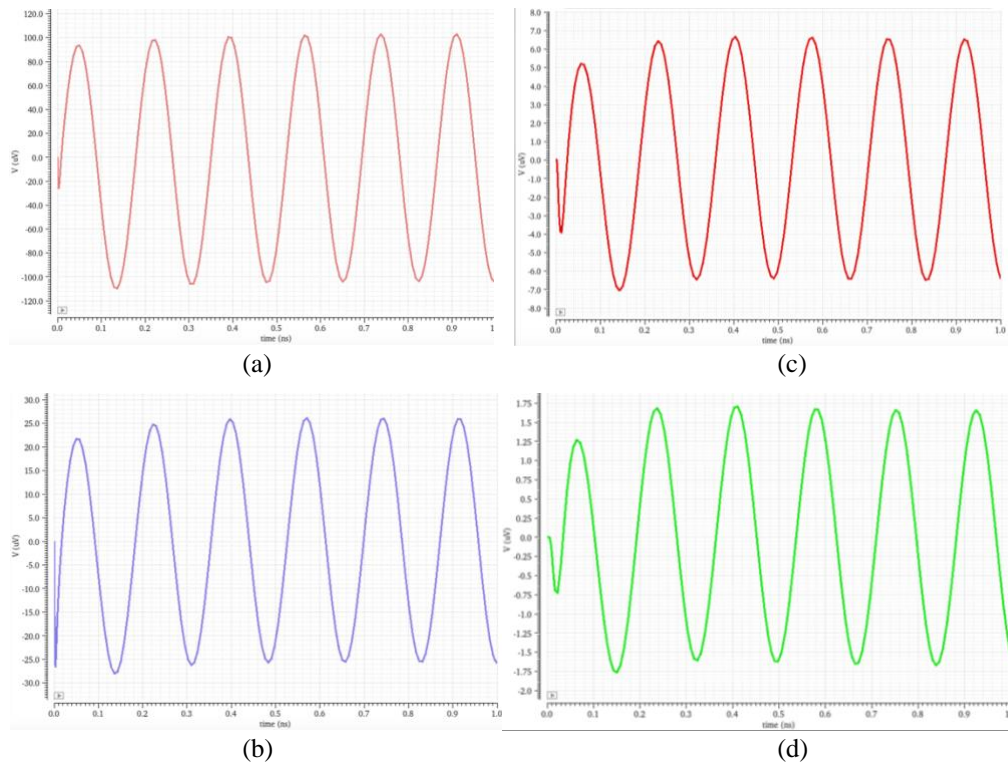


Figure 4. 13: RSSI's cascaded limiting stages output from stages 1 to 4

4.3.2. RSSI output

The output of RSSI with LPF capacitor equals 200fF is shown in Figure 4.14. Undesirable ripples exist at the output which need to be eliminated for better detection. Therefore, the LPF capacitor has been increased to 200pF which resulted in a larger delay but much smoother output. The smoother RSSI output is shown in Figure 4.15. Figure 4.16 shows that the RSSI output is saturating faster with every additional cascaded stage. This fast impulse response is a result of the linear-in-dB behavior from the proposed piece-wise logarithmic amplifier which leads to a desirable fast settling time.

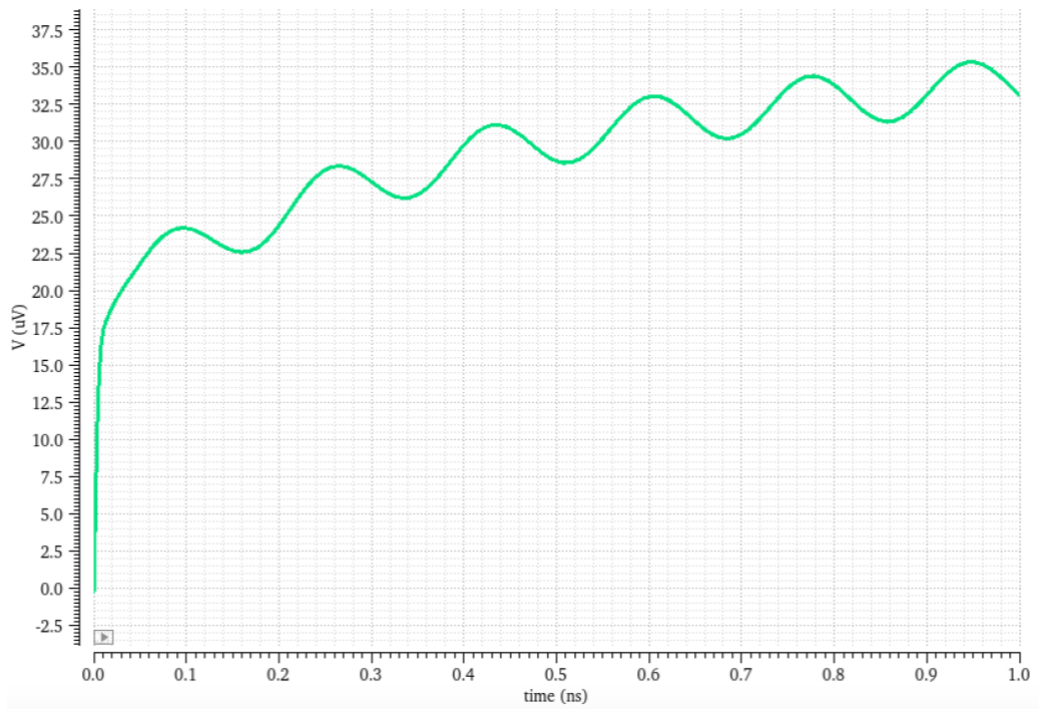


Figure 4. 14: RSSI output with ripples

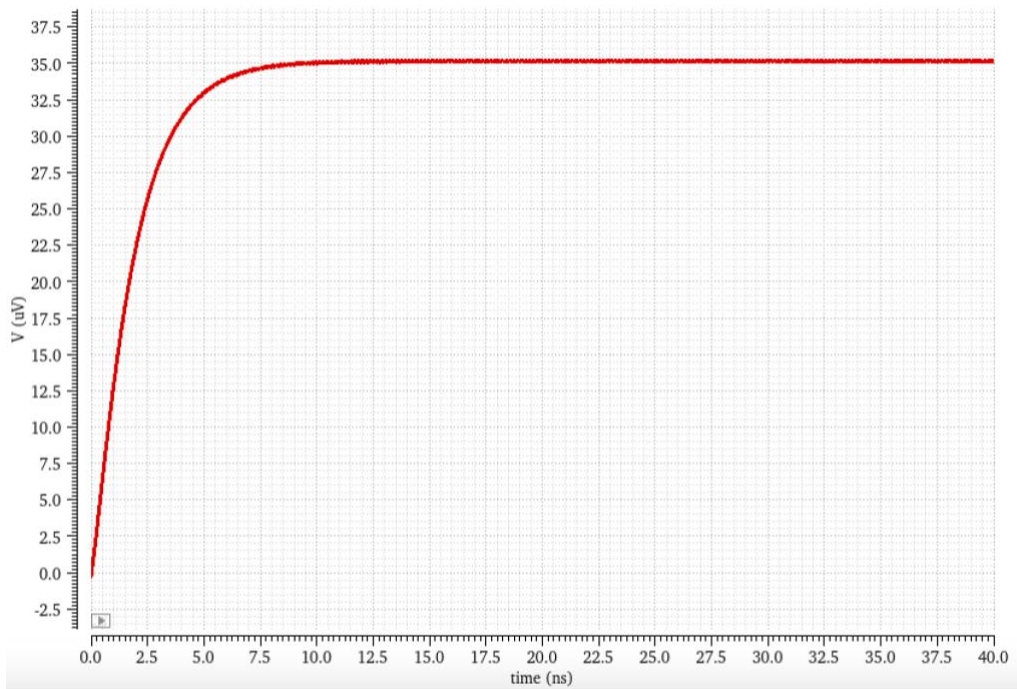


Figure 4. 15: RSSI smoother rectified output

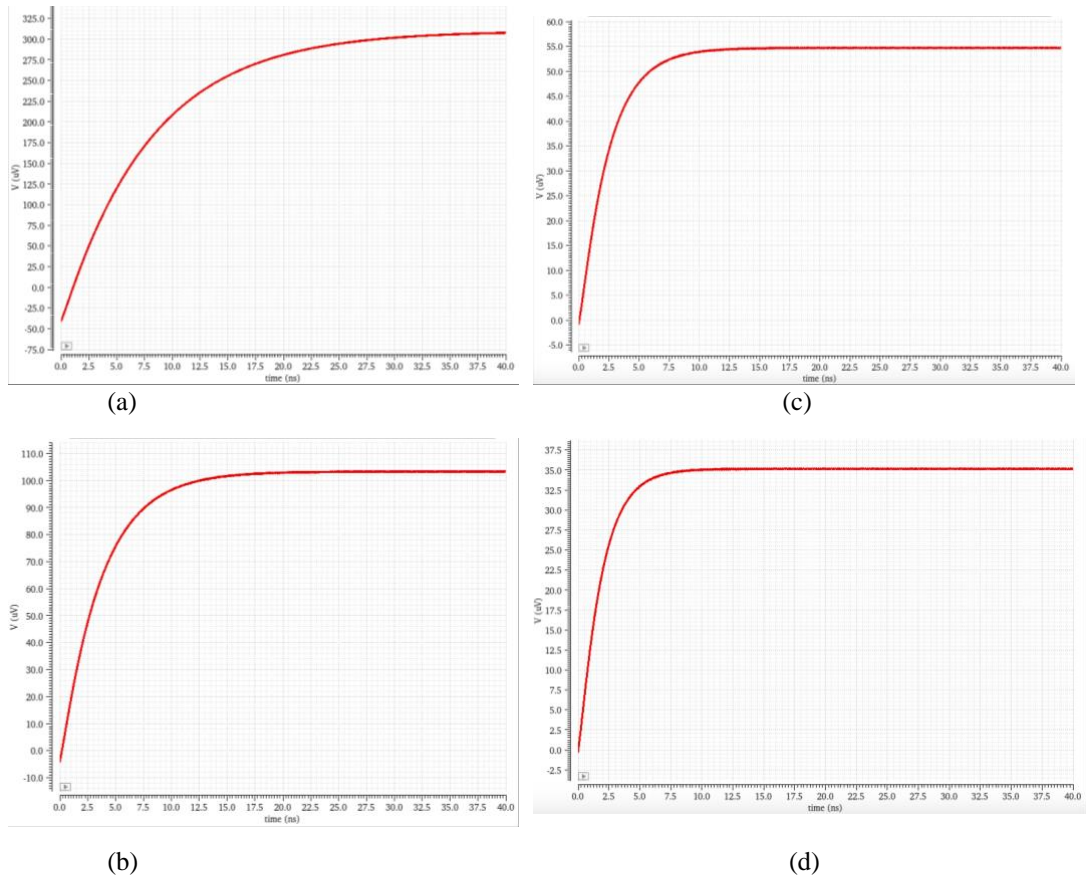


Figure 4. 16: RSSI output after each stage

4.3.3. RSSI acceptable input range

To determine the proposed RSSI acceptable input range, the input voltage has been varied. Then, the RSSI output corresponding to each varied input is observed. It can be seen from Figure 4.17 that up to 1mV input, the output is a smooth DC, then beyond that, it starts producing AC output.

4.3.4. RSSI dynamic range

To determine the dynamic range of a received signal strength indicator, the v_{out} vs. v_{in} behavior must be observed in logarithmic scale as shown in Figure 4.18 where the linear part of the plot determines the dynamic range. The larger the dynamic range, the more variety of input levels can be detected by the RSSI. The proposed RSSI can detect a range of 34 dB which is practical for the smart farm application of this thesis since the approximate range of the expected input is already known. Thus, not a significantly large area compared to the work done in the previous papers mentioned in the literature review chapter.

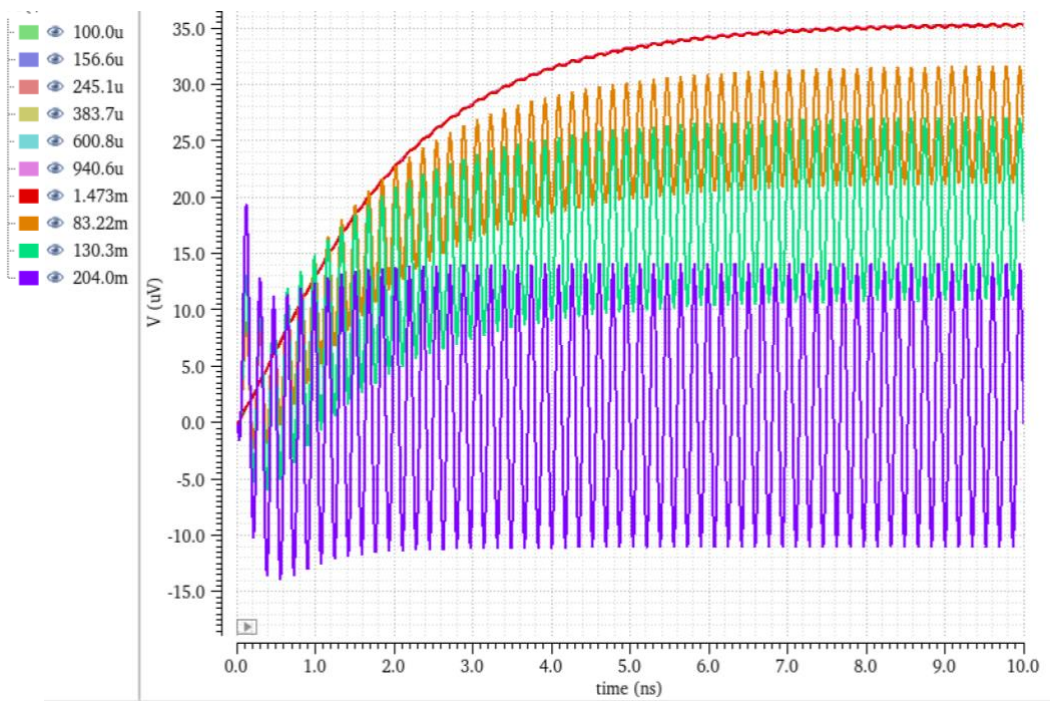


Figure 4.17: RSSI output given various input levels

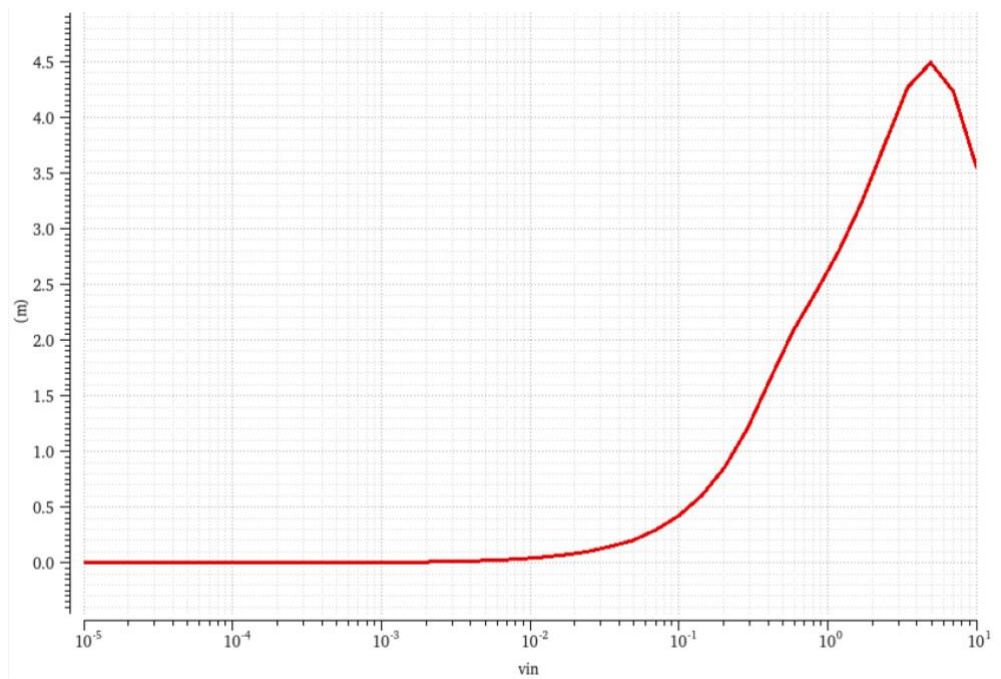


Figure 4.18: RSSI vout vs. vin logarithmically scaled

4.3.5. RSSI power consumption

All the limiting cells shown in Figure 4.12 have 1V bias on each side and there are 4 limiting differential pairs, hence, $4*2=8$ transistors. Since each of the 1V sources draws 14.68 nA, the power drawn from the rest of the bias power supplies can be calculated as $1*14.68 \text{ n} * 8 = 0.117 \text{ uW}$. In addition, the main 1V power supply draws 38 mA. Hence, the total power consumption of our RSSI system can be calculated as follows:

$$P_{consumption} = 38.35\text{m} + 0.117\text{u} = 38.35 \text{ mW}$$

4.4. Results Discussion

As observed from the simulation results, the targeted WPT 5.8GHz signal was successfully rectified even with very small amplitudes, taking into consideration the transmitter's WPT signal, the antenna gains, as well as the propagation losses. The proposed RSSI required minimal components and power, making it cost and power effective.

Initially using the Friis equation, the receiver was considered to be up to 10 m from the transmitter, however, after analyzing the system and finding out that it can detect inputs as low as 10uV and as large as 1mV, the calculation required working backward by converting our peak voltage to Vrms. Then, given input impedance is 50Ohms, the famous P squared over R formula was used to obtain the received power and then the Friis formula, equation (11), was used to identify the maximum and minimum distance the WPT receivers can be away from the transmitter while still being detectable by the proposed RSSI. It can be deduced that the WPT receiver can be as high as 500m from the transmitter and as low as 5m from the transmitter. Moreover, it can detect from -90 dBm to -50 dBm in terms of received power.

As indicated by Table 4.5, this is the first time the RSSI circuit is targeted for WPT receivers at 5.8 GHz with similar to better values of other important parameters such as sensitivity, dynamic range, power, and logarithmic error. A dynamic range of 34 dB is achieved which is lesser than the previous work, but it is due to the fact that the other designs are operating at much lower speeds. A sensitivity level of 10 μ V is achieved by the proposed system which is significantly low. The RSSI system designed in this work has a much lower logarithmic error (0.4 dB) in comparison to others but has a higher power consumption (35 mW) as the system designed is operating at a higher frequency.

Although power requirements in past literature papers are lower than the power of the proposed RSSI, 38.35 mW, but the proposed RSSI works for much higher frequencies. If one of the RSSI systems from the previous work is used for the targeted 5.8 GHz signal of this thesis, it means an RF downconverter mixer is needed which requires significantly high power as seen in the datasheet in [25] which shows an example of a high-frequency mixer for up/down conversion from the company Linear Technology. Their mixer required 558 mW which is greatly higher than the proposed RSSI system in this thesis which does not require a downconverter. Another RF active mixer is present in the datasheet in reference [26] which uses a supply voltage of 8V and a supply current that reaches 45mA leading to a power requirement of 360 mW.

Table 4. 5: RSSI performance comparison

	[6] simulated	[16] measured	[27] simulated	[28] measured	[29] measured	[30] measured	This work simulated
Frequency	0.1- 20 MHz	0.03-2.4 GHz	17 - 166 k	10.7 MHz	0.3 – 17 MHz	40 MHz	5.8 GHz
Dynamic Range	80 dB	29 - 48 dB	81.7 dB	75 dB	56 dB	56 dB	34 dB
Power	1.2-2.9 mW	30-44 mW	5.88 uW	6.2 mW	1.8 mW	9 mW	38.35 mW
Area (mm^2)	0.06	-	0.0084	0.4	0.16	0.05	-
Logarithmic Error	1.4 dB	-	2 dB	1 dB	0.5 dB	1 dB	0.4 dB
Sensitivity Level	-	18 uV	10 uV	55 uV	-	-	10 uV
Technology	65 nm	90 nm	130 nm	0.6 um	130 nm	130 nm	65 nm

Chapter 5. Conclusion and Future Work

Wireless systems have been on the rise for the past decade. Wirelessly charging drones using RF beams is a field of interest these days as it allows for longer charging distances and can operate in harsh weather conditions. This thesis proposed a high-precision RSSI using CMOS 65 nm technology that allows the WPT transmitter to charge moving drones in the air by detecting the signal to ensure continuous coverage and localization. In this thesis, an RSSI system using TSMC CMOS 65 nm is designed and investigated for a wireless power transfer receiver. It can be concluded that the proposed RSSI design is an ideal choice due to its low power consumption, high sensitivity, and linear-in-dB behavior. This work successfully rectified the targeted WPT signal at 5.8 GHz even with very small amplitudes showing a high sensitivity level of as low as 10 μV , power consumption of 38.35 mW, a dynamic range of 34 dB, and logarithmic error of 0.4 dB taken, into consideration the transmitter's WPT signal, the antenna gains, as well as the propagation losses. In the future, the designed RSSI circuit can be fabricated. The RSSI system can be implemented for real-time localization. Moreover, programmable reference bias currents can be used for the rectifiers to control the tradeoff between the dynamic range and detection sensitivity of RSSI.

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Vita

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