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CHIP LEVEL IMPLEMENTATION OF A DIGITAL
RADAR SYSTEM

by

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A Thesis Presented to the Faculty of the
American University of Sharjah
College of Engineering
in Partial Fulfillment
of the Requirements
for the Degree of

Master of Science in
Electrical Engineering

Sharjah, United Arab Emirates

May 2015

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Acknowledgements

First of all I would like to thank Allah, the most gracious most merciful for His unlimited gifts. I would like to thank my lovely parents and family for their endless help, support and patience. Also, I would like to sincerely thank my brilliant mentors and advisors; Dr. Lutfi Albasha and Dr. Hasan Mir who taught, helped and guided me patiently during the process of writing my thesis. My deepest thanks go to Dr. Nasir Quadir and Eng. Ibrahim Abusaif for their technical advice. I also appreciate the tremendous support I got from the Department of Electrical Engineering at the *American University of Sharjah* for sponsoring my M.Sc degree studies. I would like to thank AWR corporation for providing me with one year free license for AWR design environment package. Finally, I would like to thank all my friends and colleagues for their support and encouragement.

Dedication

*... To my mother who taught
me how to hold the pen ...*

Abstract

In this work, an S-Band radar system based on stretch processing technique is developed at chip level. The novelty in this work lies in providing an integrated, compact and miniaturized radar system chipset. The radar has many characteristics that ensure high performance: a wide bandwidth signal (600 MHz) that provides high resolution to distinguish between close objects, stretch processing technique that dramatically reduces the required sampling rates and relaxes the specifications of analog to digital converters, high dynamic range that allows weak signals to be detected from targets masked by high levels of clutter (such as snow and rain), multiple receiver channels that enable digital antenna beam forming at the receiver to mitigate any strong interferer, and finally operation in the S-Band (2-4 GHz) that provides high immunity against clutter in long range surveillance applications. The architecture study revealed a Super-Hetrodyne receiver and modulator architecture offered the best solution. The high order filters were pushed off chip to reduce silicon area, reduce power consumption and improve filtering results. The circuit level design focused on designing the receiver blocks. The design included a high linearity quad passive mixer, IF cascode and common source amplifiers, and a negative gm voltage controlled oscillator. The total receiver system of the radar chipset was designed and simulated at the circuit level using Cadence Virtuoso 6.0 on IBM 180 nm CMOS technology, a high dynamic range of 58 dB was achieved with a total power consumption of 0.32 W.

Search Terms: Stretch processing; S-Band transceiver; High resolution radar; High dynamic range radar; Quad passive mixer; negative gm voltage controlled oscillator.

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Abbreviations

SFDR	Spurious Free Dynamic Range
NF	Noise Figure
IF	Intermediate Frequency
IIP2	Input Second Order Intercept Point
IIP3	Input Third Order Intercept Point
RFIC	Radio Frequency Integrated Circuits
P1-dB	Input 1 dB Compression Point
PN	Phase Noise
C/N	Carrier to Noise Ratio

Chapter 1: Introduction

1.1 Problem Statement

In the last decade, radar technology and applications have been expanding continuously. Moreover, the demand for high performance, low cost and efficient radars is increasing [1]. Radars are usually characterized by their resolution (the ability to distinguish between close objects) [2], as well as their ability to function properly in the presence of noise, clutter and jammers. Radar resolution depends mainly on the radar waveform spectral bandwidth, since higher bandwidth waveforms provide higher resolution performance. On the other hand, high bandwidth signals require sophisticated and fast analog to digital converters. The introduction of stretch processing technique was a solution to this issue. Stretch processing radars maintain high resolution while at the same time reducing the baseband spectral bandwidth [3], [4], thus reducing the analog to digital converters sampling rates.

In addition to the need for high performance functional equipment, the size of the equipment along with its portability and battery life are significant factors in rating any equipment. This work focuses on the design and implementation of a portable miniaturized integrated radar system chipset. The radar system uses stretch processing technique, and operates in the S-Band. In addition to the integration of the radar at the chip level, it possesses many desirable qualities, such as high dynamic range, high resolution, and high immunity against clutter in long range applications.

1.2 Thesis Organization

In chapter two, a brief background about the basic concepts of radars is provided. Chapter three illustrates the concept of stretch processing and digital beamforming. Then, chapter four provides an introduction to the most prevalent nomenclatures encountered in radio frequency integrated circuits systems design. In chapter five, a detailed system level design and simulation is developed for the proposed radar system. Chapter six shows the circuit level design and simulation of the receiver system blocks, which includes a quad passive mixer, negative gm voltage controlled oscillator and cascode amplifier circuits. Chapter seven shows the complete simulation of the receiver system at the circuit level. Finally, chapter eight sums up the conclusion of the thesis and discusses the potential future work.

Chapter 2: Introduction to Radar Systems

2.1 Detection Radar Basic Principle of Operation

In its simplest form a radar radiates electromagnetic waves in all directions, once an electromagnetic wave hits an object it will be reflected back as shown in Figure 1. These reflected waves are usually called echo waves or echo signals. The radar's receiver is responsible for detecting these echo signals and providing accurate information such as speed, location, etc. [5], [6].

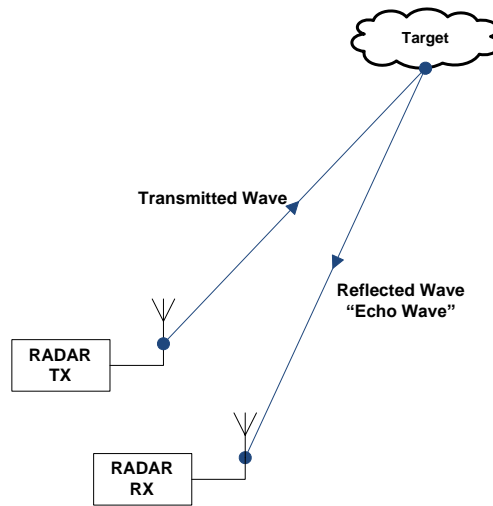


Figure 1: Basic detection radar principle of operation

The electromagnetic wave will travel a distance R from the transmitter to the object, and the same distance back from the object to the transmitter, thus covering a total distance of $2R$. Since electromagnetic waves travel in space at the speed of light, the distance R can be calculated directly using equation (1).

$$R = \frac{c T_R}{2} \quad (1)$$

where c is the speed of light, and T_R is the time elapsed between transmitting the signal and receiving its echo. The distance R is usually called the range of the target.

2.2 Radar Classifications and Performance Metrics

Radars are classified based on the waveform they transmit, either as continuous wave radars or as pulsed radars [7]. In continuous wave radars the radar is continuously transmitting a wave while it is receiving at the same time. On the other hand, pulsed radars transmit a pulse for a certain period of time, and then switch into receiving mode for a specific period of time. A total amount of time called the pulse repetition period, T_p , should elapse between the transmission of two consecutive pulses. Pulsed radars tend to be more popular than continuous wave radar [7].

Radar performance is described in terms of many factors. Some of the most common metrics are resolution and maximum range. Resolution is the minimum distance between two adjacent objects for which the radar is capable of distinguishing these two objects from each other (i.e. not considering them as a single object). The maximum range, as its name implies, is the maximum distance from the radar for which a target can be detected [5].

The resolution of the radar depends mainly on the pulse width. As the pulse extends in time τ_p seconds, it extends an equivalent distance of $c\tau_p$ in space. From this simple fact, it can be shown that the resolution is as given by equation (2).

$$\Delta R = \frac{c\tau_p}{2} \quad (2)$$

The division by two is due to the two way travel of the signal (from radar transmitter to target and back from target to the radar receiver). Equation (2) shows that lower pulse width achieves higher resolution, consequently, if the pulse is more confined in time domain the bandwidth of its equivalent spectrum in frequency domain is higher. Therefore, it can be alternatively said that higher bandwidth pulses provides better resolution [6].

The radar's maximum range is governed by the radar range equation [5], which relates the range to the transmitter, receiver, antenna, target and environmental characteristics. The equation is given by:

$$R_{\max} = \frac{P_t G A_e \sigma}{(4\pi)^2 S_{\min}} \quad (3)$$

where:

R_{\max}	:	Maximum range
P_t	:	Transmitted power
G	:	Antenna gain
σ	:	Target cross section
A_e	:	Antenna effective area
S_{\min}	:	Minimum detectable power level at the receiver

- Target cross section σ determines the portion of reflected power from the target surface back to the radar's receiver (σ depends mainly on the target shape) [8].
- $A_e = \rho \cdot A$, where A is the physical aperture area and ρ is the antenna aperture efficiency.

A detailed derivation of the radar equation in its simplest form can be found in [5]. Also the radar equation can be modified to account for wideband signals, a good reference for ultra wideband signals radar equation is provided in [9]. Qualitatively, the radar equation shows that higher transmitted power achieves higher range distance. Also a good antenna design with good gain and effective area enhances the radar's range. The sensitivity of the receiver plays significant role in determining the range; the better the sensitivity, the higher the range of the radar.

As the environment of operation is not free of impairments and noise, a signal level detection threshold is usually assigned. The detection threshold role is to distinguish between real echo signals and other irrelevant signals including noise. So any signal having lower power level than the threshold level will be neglected and won't be considered as an echo signal (i.e. target). This concept is illustrated in Figure 2.

Another important point to emphasize is that after transmitting a pulse, sufficient time before transmitting the next pulse should elapse, otherwise, the echo signal will return back during the next pulse duration, and be erroneously translated as the echo of the next pulse (called second time around echo), thus leading to wrong range information about the target.

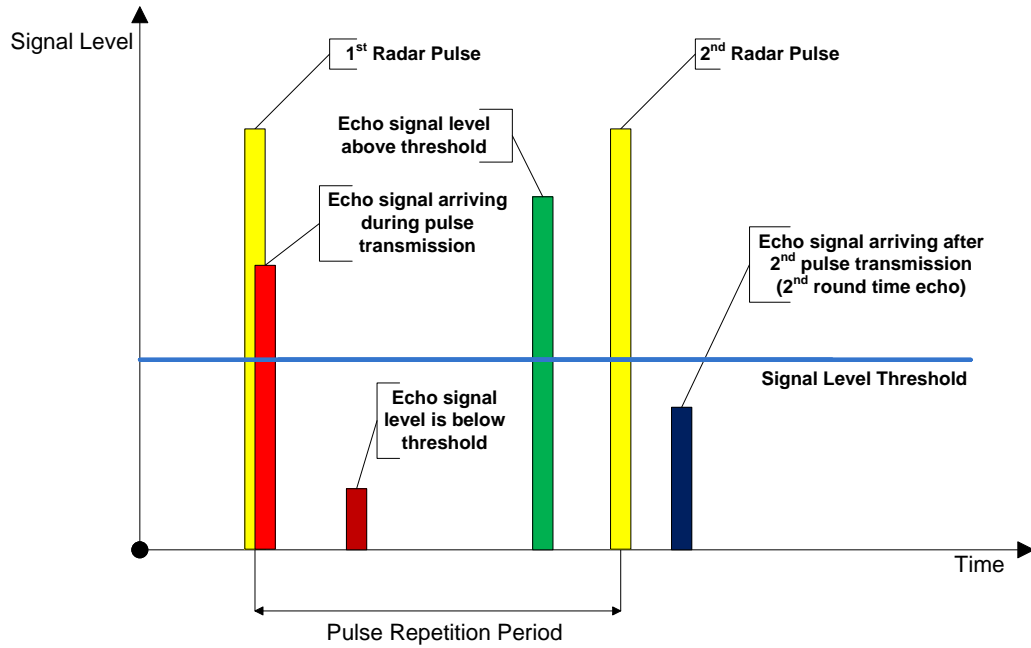


Figure 2: Various scenarios of pulsed radar echo signals

The pulse repetition period determines a very important performance factor, which is the maximum unambiguous range. Hence, choosing consistent values for transmitted power and pulse repetition period eliminates the appearance of multiple around time signals above the signal level threshold [5].

Radar systems can also be classified based on the location of the transmitter and receiver [10]. For example, if the radar has its transmitter and receiver located at the same place, it is classified as a Monostatic radar. However, if its transmitter and receiver are located at different places, it's considered a Bistatic radar. Monostatic radars are more common and have less complexity than Bistatic ones [10]. Another type is the Multistatic radar, in which there are different transmitters and receivers located at different places. Radar systems may also be classified based on their functionality (detection, search, tracking, etc.) [5].

Chapter 3: Stretch Processing and Digital Beamforming

3.1 Stretch Processing

As previously mentioned in Chapter 2, the resolution of the radar is an important factor in determining the performance quality of the radar. Higher bandwidth waveforms provide better resolution. However, processing high bandwidth signals in the digital domain requires high sampling rates for analog to digital converters according to Nyquist theorem [11]. Stretch processing technique provides high resolution performance, while at the same time maintaining relatively low bandwidth, dramatically reducing sampling rates requirement.

Stretch processing uses chirp signal as the radar pulse waveform. The chirp is simply a linear frequency modulated signal (LFM), and can be generated by an FM modulator along with a linear input signal. A sawtooth signal will provide repetitive sequence of chirps based on the sawtooth period. The process of chirp generation is shown in Figure 3.

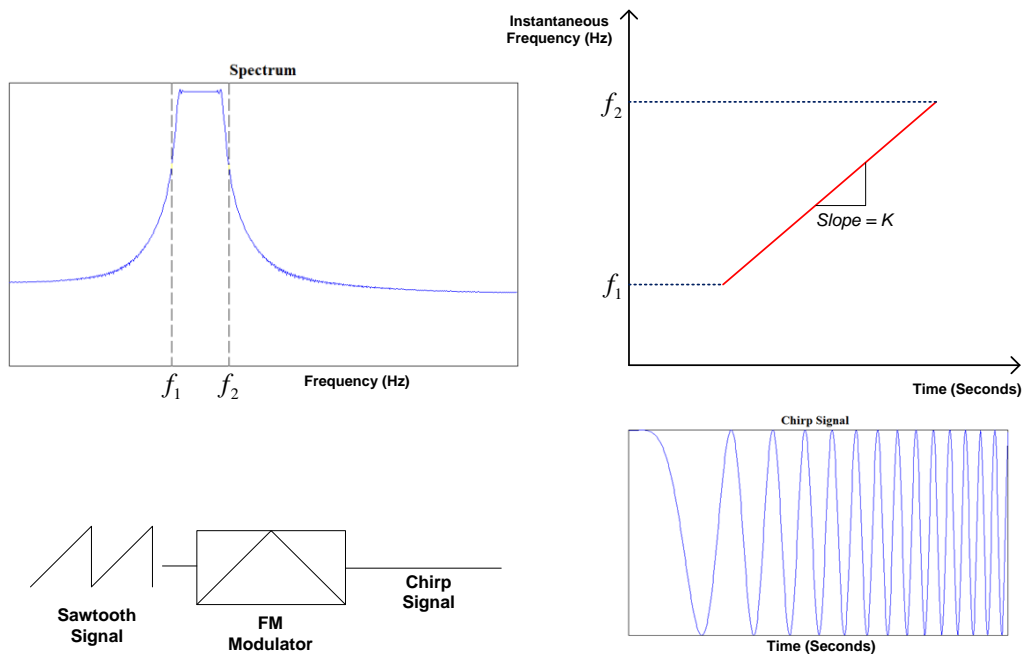


Figure 3: Chirp signal generation, spectrum and time domain waveform

Assuming $m(t) = t \cdot u(t)$ as the input signal to the FM modulator, the FM modulator output can be written as:

$$\phi_{FM}(t) = A \cos(2\pi \cdot (f_c t + k \int_{-\infty}^t m(t) \cdot dt)) \quad (4)$$

$$\phi_{FM}(t) = A \cos(2\pi \cdot (f_c t + k \int_0^t t \cdot dt)) \quad (5)$$

$$\phi_{FM}(t) = A \cos(2\pi \cdot (f_c t + \frac{kt^2}{2})) \quad (6)$$

where f_c is the carrier frequency in Hz, k is the sensitivity of the FM modulator in Hz/V (i.e. how much frequency shift in Hz will be produced by 1 V change in the input level).

As the frequency is equal to the time derivative of the cosine argument, the instantaneous frequency can be written as given by equation (8):

$$f(t) = \frac{1}{2\pi} \cdot \frac{\partial}{\partial t} (2\pi \cdot (f_c t + \frac{kt^2}{2})) \quad (7)$$

$$f(t) = f_c + kt \quad (8)$$

Equation (8) shows that the instantaneous frequency changes linearly with time with a slope of k Hz/V. Moreover, in the frequency domain, the chirp spectrum appears to be confined between the lowest and highest instantaneous frequencies. The factor k can also be interpreted as the chirp spectral bandwidth to temporal chirp duration ratio:

$$k = \frac{\Delta B}{\Delta T} \quad (9)$$

where, ΔB is the spectral bandwidth of the chirp and ΔT is the temporal duration of the chirp.

A chirp signal can be used to provide a flat high bandwidth spectrum. Now assuming that a chirp is used as the radar signal waveform $S_{TX}(t)$, and assuming that another chirp signal $S_{LO}(t)$ with the same bandwidth is provided at the receiver local oscillator.

$$S_{TX}(t) = \cos(2\pi \cdot (f_{TX}^0 t + \frac{kt^2}{2})) \quad (10)$$

$$S_{LO}(t) = \cos(2\pi \cdot (f_{LO}^0 t + \frac{kt^2}{2})) \quad (11)$$

$$S_{RX}(t) = S_{TX}(t - \tau) = \cos(2\pi \cdot (f_{TX}^0 (t - \tau) + \frac{k(t - \tau)^2}{2})) \quad (12)$$

The radar's received echo signal is a delayed version of the transmitted signal $S_{RX}(t) = S_{TX}(t - \tau)$.

Mixing $S_{RX}(t)$ with $S_{LO}(t)$ and bandpass filtering the output (This operation is usually denoted as deramping) [4] results in:

$$S_o(t) = BPF(S_{RX}(t) \cdot S_{LO}(t)) = \cos(2\pi \cdot ((f_{TX}^0 - f_{LO}^0) + k \cdot \tau)t + \frac{k\tau^2}{2} - f_{TX}^0 \tau) \quad (13)$$

As equation (13) shows, the output is a tone with frequency proportional to the delay τ of the echo signal ($f_o = (f_{TX}^0 - f_{LO}^0) + k\tau$), thus proportional to the target range. The bandpass filter is centered at $(f_{TX}^0 - f_{LO}^0)$ and its bandwidth defines the range window (i.e. minimum and maximum range) [12]. The deramping process is shown in Figure 4.

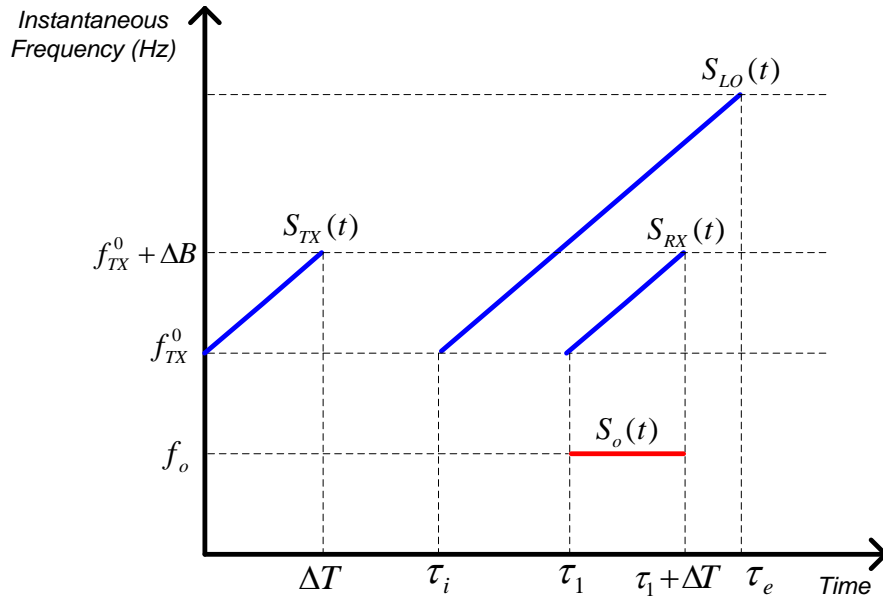


Figure 4: Graphical representation of deramping operation

To calculate the radar resolution after using stretch processing, it can be seen from equation (13) that the frequency resolution is:

$$\Delta f = k \cdot \Delta \tau \quad (14)$$

where $\Delta \tau$ is the time resolution, which is also proportional to the spatial resolution.

Assuming pulse duration of T seconds, the frequency resolution is the inverse of the pulse duration, which is the bandwidth of its spectrum (i.e. Sinc function).

$$\Delta f = \frac{1}{T} \quad (15)$$

$$k = \frac{B}{T} \quad (16)$$

Substituting equation (16) in (14) and equating (15) with (14) results in:

$$\frac{B}{T} \cdot \Delta \tau = \frac{1}{T} \quad (17)$$

$$\Delta \tau = \frac{1}{B} \quad (18)$$

Hence:

$$\Delta R = \frac{\Delta \tau \cdot c}{2} \quad (19)$$

Substituting equation (18) in (19) results in

$$\Delta R = \frac{c}{2B} \quad (20)$$

As expected, equation (20) shows that the resolution increases by having higher bandwidth. The strength of stretch processing technique lies in providing a high bandwidth waveform that ensures high resolution, while allowing the received signal to be "deramped" to produce tones that have lower bandwidth, and thus reducing the analog to digital converters sampling rates requirements [12].

3.2 Beamforming and Linear Array Processing

In different practical situations the received signal is corrupted by many other undesired signals. The main task of the receiver is to provide high selectivity to

extract the desired signal from all other undesired ones. These undesired signals are often intentional jamming signals that are received from certain directions. Using an array of antennas at the receiver side, along with an array processing algorithm can identify the signals direction of arrival and mitigate the effect of jamming signals [13].

Figure 5 shows a uniform linear antenna array of N antennas. The received signal from a certain direction ϕ will have to travel an extra distance of $d \sin(\phi)$ from antenna 1 to antenna 2, and the same extra distance from antenna 2 to antenna 3, and so on. This extra propagation distance is translated as a time delay in each antenna output. Based on the assumption that the wave is propagating at the speed of light c , the delay at the n^{th} antenna can be given by equation (21).

$$\tau_N = \frac{(N-1) \cdot d \sin(\phi)}{c} \quad (21)$$

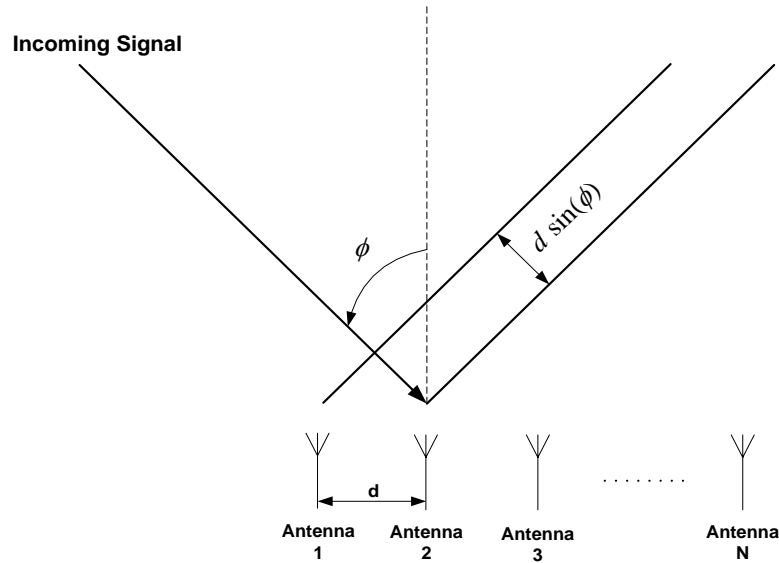


Figure 5: Uniform linear antenna array of N antennas

Assuming that the incoming high frequency signal has already been demodulated to baseband using a typical IQ demodulator, and converted to a digital signal as shown in Figure 6, the output of each antenna $x_N(n)$ will be delayed by the

value τ_N . By knowing the value of τ_N , the angle of arrival ϕ can be easily found from equation (21).

Converting the time delays in time domain into phase shifts in frequency domain, results in a useful vector known as the steering vector. The steering vector describes the gain of the linear antenna array to a signal coming from a certain direction. The steering vector is given by equation (22) and the receiver output is given by equation (23) [14].

$$v(\phi) = [1 \quad e^{-j2\pi f_c \tau_2(\phi)} \quad \dots \quad e^{-j2\pi f_c \tau_n(\phi)}] \quad (22)$$

$$s(k) = v(\phi) \cdot x^t(k) \quad (23)$$

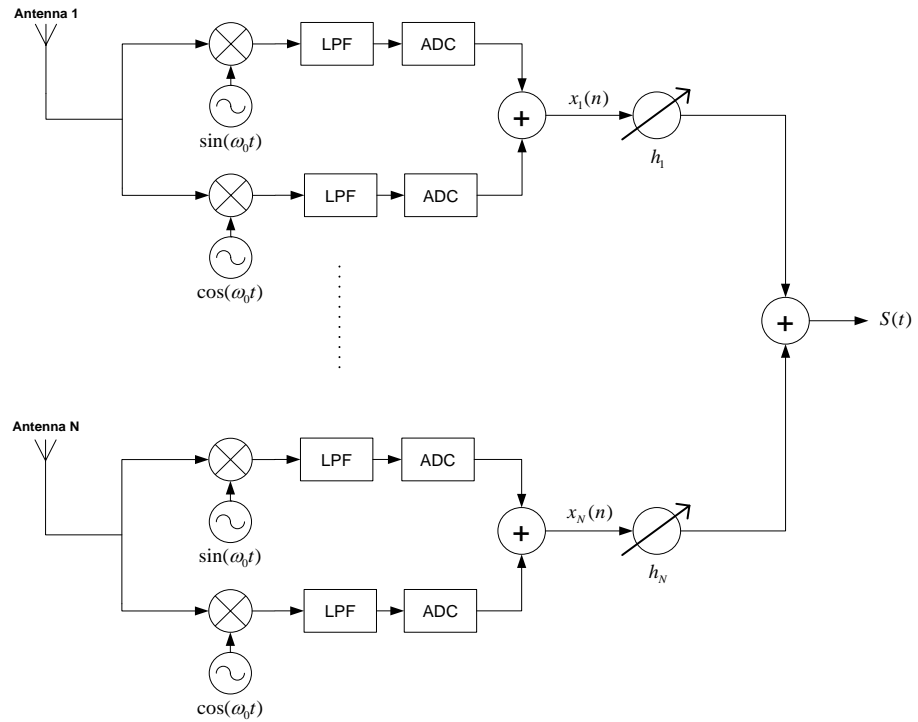


Figure 6: Linear array IQ demodulator with beamforming weight factor (h)

Another important quantity is the spatial correlation of the array, defined by equation (24). Based on the assumption that the statistical average is equal to the time average (i.e. Ergodic Process), equation (24) can be approximated using equation (25).

$$R_x = E [x \cdot x^t] \quad (24)$$

$$R_x = \frac{1}{K} \sum_{k=1}^K x(k) \cdot x'(k) \quad (25)$$

The spatial correlation matrix size is (N x N), where N is the number of antennas in the array. The eigenvectors corresponding to the signal (both desired and undesired) form the signal subspace, whereas the remaining eigenvectors form the noise subspace u_w .

For the signal angles of arrival ϕ_n , it can be shown that [14]:

$$u_w \cdot v(\phi_n) = 0 \quad (26)$$

Equation (26) is useful in determining the angles of arrival, since a search over possible angles of the inverse of (26) will yield infinite or relatively large value in practical scenarios.

By knowing the direction of arrival of the desired signal, the output can be optimized by multiplying the steering vector by another weighting vector h . The value of h is chosen in a way to maximize the receiver gain for the desired angle and reject other interference angles. Equation (27) shows the result of solving the optimization problem for maximizing the gain of the desired signal incident from an angle ϕ_n while at the same time minimizing the gain for other incident angles [14].

$$h = R_x^{-1} \cdot v(\phi_n) \quad (27)$$

Figure 7 shows a simple example where there are three incident signals with three different angles (-40, 0 and 40 degrees). The green waveform refers to the output of the receiver in normal situation where no beam forming is applied.

As mentioned previously, a weighting vector h can be applied at the receiver to maximize the gain for a certain angle and minimize it for other angles. Figure 8 shows the detected angles of arrival. Figure 9 shows the linear antenna array gain after applying a weighting vector to maximize the gain for the second signal incident at 0 degrees. As expected the figure shows that the gain goes to 0 at the undesired angles (-40 and 40 degrees) and has a maximum at the desired angle (0 degrees). Figure 10 shows that the receiver output in time domain is identical to the desired signal (Second Signal). The MATLAB Code for this example is available at Appendix A.

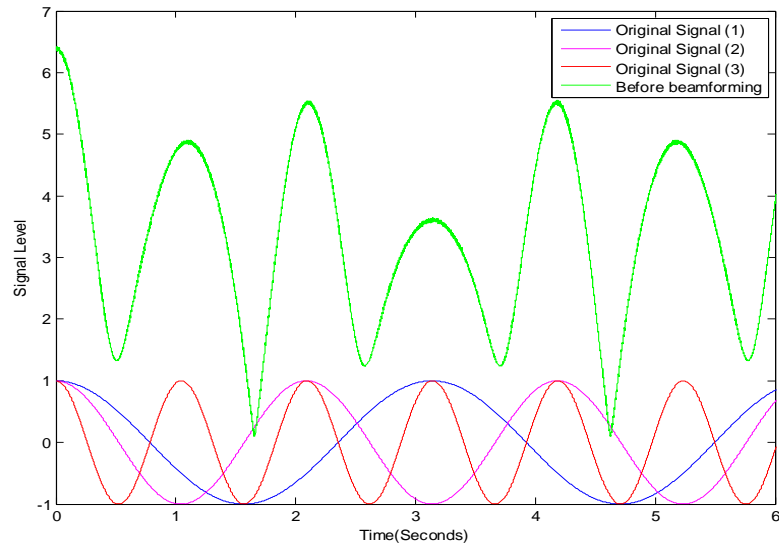


Figure 7: Waveforms of three received signals at different angles (red, blue and pink) and receiver output without applying beamforming (green)

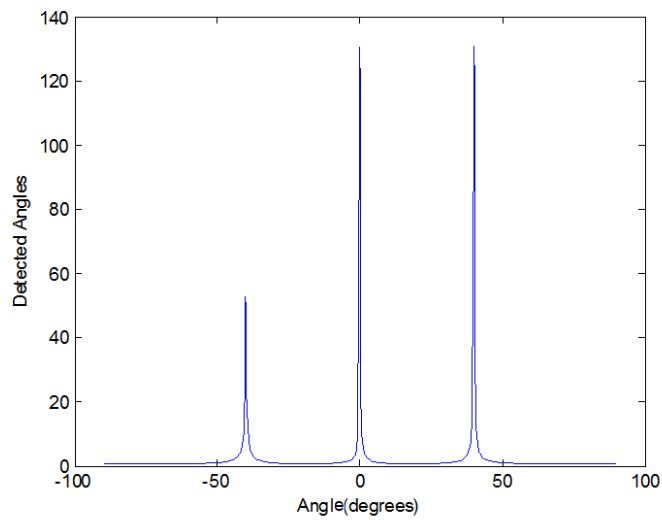


Figure 8: Detected angles of arrival

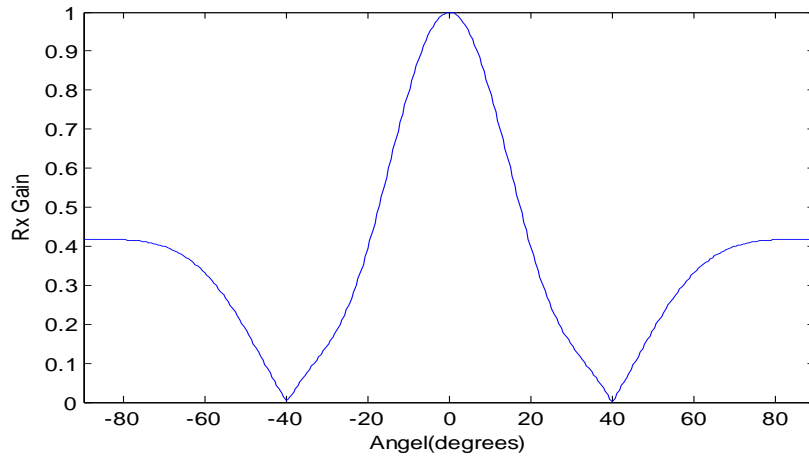


Figure 9: Linear antenna array gain

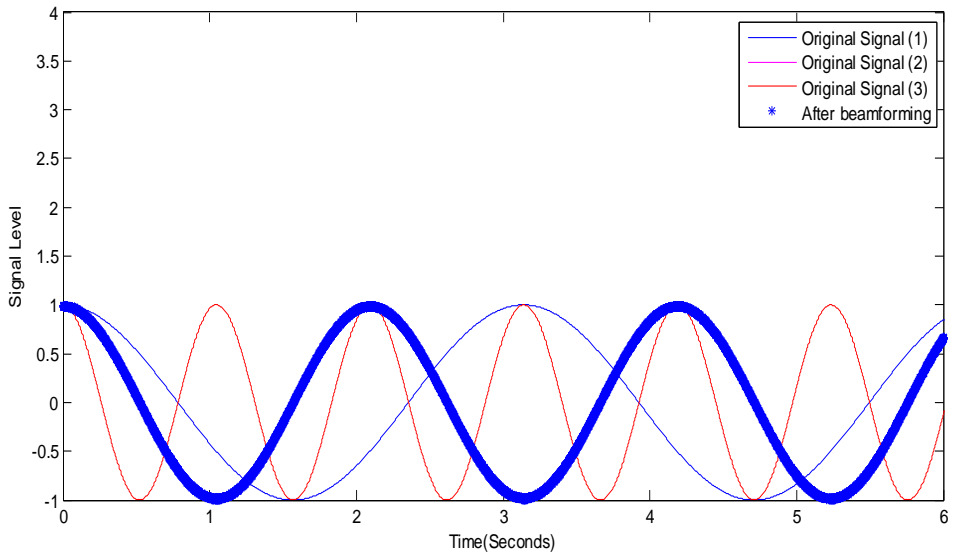


Figure 10: Receiver output after beamforming

Chapter 4: Radio Frequency Integrated Circuits System Design Aspects

4.1 Introduction

In the analysis of communication systems, it's usually assumed that the system blocks are ideal. For example an amplifier is considered a perfect linear and noiseless stage that only multiplies the incoming signal with a certain gain factor, while a mixer is considered a perfect multiplier and so on. However, when it comes to realizing a practical system, especially at radio frequencies, many physical limitations and non idealities are encountered. Therefore, designing an RFIC system mandates including many non ideal effects in the system level analysis and design. This section provides brief overview of the main issues encountered in RFIC systems design. There are primary issues included but are not limited to nonlinearity effects, noise and non ideal filtration [15], [16], [17].

4.2 Nonlinearity Effects

In its simplest form a linear system can be described mathematically by:

$$y(t) = a \cdot x(t) \quad (28)$$

Equation (28) represents the ideal behavior of an amplifier, in which a is the amplifier gain. However, real circuits are made of devices that have physical limitations which result in a nonlinear behavior that can be described by Taylor series expansion. In general, truncating the series at the third term is sufficient to provide a good model.

$$y(t) = a_1 \cdot x(t) + a_2 \cdot x^2(t) + a_3 \cdot x^3(t) \quad (29)$$

Assuming the input is $x(t) = A\cos(\omega t)$, the linear output is expected to be $y(t) = a \cdot A\cos(\omega t)$, however, due to saturation and nonlinear behavior of the amplifier the output becomes:

$$y(t) = a_1 \cdot A\cos(\omega t) + a_2 \cdot (A\cos(\omega t))^2 + a_3 \cdot (A\cos(\omega t))^3 \quad (30)$$

$$y(t) = \frac{a_1 A^2}{2} + (a_1 A + \frac{3a_3 A^3}{4})\cos(\omega t) + \frac{a_2 A^2}{2}\cos(2\omega t) + \frac{a_3 A^3}{4}\cos(3\omega t) \quad (31)$$

As is obvious from equation (31), new harmonics were generated at the amplifier output due to its nonlinear behavior. The effect of generating harmonics is usually referred to as harmonic distortion, second order and third order harmonic distortions are usually described by the second and third harmonic power levels compared to the fundamental [18].

4.3 Intermodulation

Intermodulation is another effect of nonlinearity. Assuming the input is given by equation (32):

$$x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \quad (32)$$

Applying the input given by equation (32) to the nonlinear system given by equation (29), results in the output given by equation (33):

$$y(t) = a_1 \cdot (A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)) + a_2 \cdot (A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t))^2 \dots \quad (33) \\ \dots + a_3 \cdot (A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t))^3$$

Expanding equation (33) will result in frequency components centered at $(\omega_1 \pm \omega_2)$, $(2\omega_1 \pm \omega_2)$ and $(2\omega_2 \pm \omega_1)$. These components are called intermodulation products. They are so named from the effect of internally modulating the frequency components of the same signal for each other (i.e. as if $A_1 \cos(\omega_1 t)$ has modulated $A_2 \cos(\omega_2 t)$ and vice versa). Table 1 shows the coefficients of each component after expanding equation (33) .

System nonlinearity produces new components in the frequency domain. These components can affect adjacent channels and produce the so called adjacent channel interference. In designing transmitters, adjacent channel interference is a major concern. Transmitters should operate in their assigned frequency bands without interfering with other channels. Additionally, third order intermodulation products appear close to the band of interest, therefore, high level third order intermodulation products will require sharper filters to suppress them [18].

Table 1: Second and third order intermodulation products

Fundamental Components ω_1, ω_2	$(a_1 A_1 + \frac{3}{4} a_3 A_1^3 + \frac{3}{2} a_3 A_1 A_2^2) \cdot \cos(\omega_1 t)$ $(a_2 A_2 + \frac{3}{4} a_3 A_2^3 + \frac{3}{2} a_3 A_2 A_1^2) \cdot \cos(\omega_2 t)$
2 nd Order Intermodulation Products $(\omega_1 \pm \omega_2)$	$(a_2 A_1 A_2) \cdot \cos((\omega_1 + \omega_2) \cdot t) + (a_2 A_1 A_2) \cdot \cos((\omega_1 - \omega_2) \cdot t)$
3 rd Order Intermodulation Products $(2\omega_1 \pm \omega_2), (2\omega_2 \pm \omega_1)$	$(\frac{3a_3 A_1^2 A_2}{4}) \cdot \cos((2\omega_1 + \omega_2) \cdot t) + (\frac{3a_3 A_1^2 A_2}{4}) \cdot \cos((2\omega_1 - \omega_2) \cdot t)$ $(\frac{3a_3 A_2^2 A_1}{4}) \cdot \cos((2\omega_2 + \omega_1) \cdot t) + (\frac{3a_3 A_2^2 A_1}{4}) \cdot \cos((2\omega_2 - \omega_1) \cdot t)$

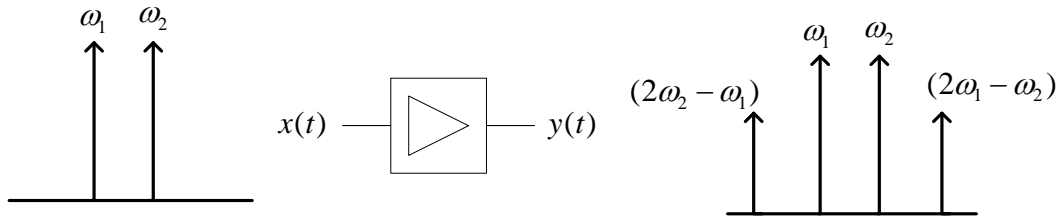


Figure 11: Nonlinear system third order intermodulation products

4.4 Receiver Desensitization

Another nonlinearity effect is the receiver desensitization, which happens when the receiver receives a desired weak signal along with a strong interferer in a nearby frequency, which eventually can reduce the gain of the desired signal to zero. This can be shown mathematically as follows:

Assuming an input $x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$, where $A_1 \cos(\omega_1 t)$ is the desired weak signal, and $A_2 \cos(\omega_2 t)$ is the strong interferer signal. The output can be written as in equation (34).

$$y(t) = (a_1 A_1 + \frac{3}{4} a_3 A_1^3 + \frac{3}{2} a_3 A_1 A_2^2) \cdot \cos(\omega_1 t) + \dots \quad (34)$$

Since $A_2 \gg A_1$, $y(t)$ can be reduced to equation (35).

$$y(t) = (a_1 A_1 + \frac{3}{2} a_3 A_2^2) \cdot \cos(\omega_1 t) + \dots \quad (35)$$

For negative values of a_3 , the gain of $A_1 \cos(\omega_1 t)$ starts to decrease and can reach zero at a certain point. This is referred to as receiver blocking or desensitization [18].

4.5 1-dB Compression Point and Third Order Intercept Point

Two common figures of merit that are used in RFIC systems to describe nonlinearity are the 1-dB compression point and the third order intercept point [17].

The 1-dB compression point is simply defined as the point for which input power results in fundamental component power gain reduction of 1-dB from the extrapolated theoretical gain. Figure 12 shows graphical illustration of the input 1-dB compression point. The input 1-dB compression point can be calculated easily as follows:

$$20 \log \left| a_1 + \frac{3a_3 A_{1-dB}^2}{4} \right| = 20 \log |a_1| - 1 \text{ dB} \quad (36)$$

$$A_{1-dB} = \sqrt{0.145 \left| \frac{a_1}{a_3} \right|} \quad (37)$$

The third order intercept point is simply defined as the point at which the third order intermodulation products level equals the fundamental component level. It is usually measured using two tone test, mathematically the input third order intercept point can be written as equation (38).

$$A_{IP3} = \sqrt{\frac{4}{3} \left| \frac{a_1}{a_3} \right|} \quad (38)$$

Figure 13 shows graphical illustration of the third order intercept point. A fast rule of thumb for calculating the third order intercept point power level of cascaded

system blocks is to add them as if they were parallel resistors as given by equation (39a). Also, equation (39b) shows the relation between the third intercept point and the 1 dB compression point.

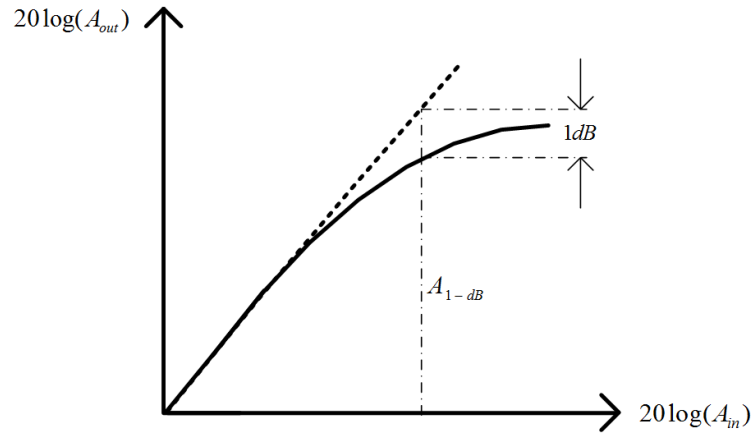


Figure 12: Input 1-dB compression point

$$IIP_3 \text{ (dBm)} \approx 10 \log_{10} \left(\frac{1}{\frac{1}{IP_{3_1}} + \frac{1}{IP_{3_2}} + \frac{1}{IP_{3_2}} + \dots} \right) \quad (39a)$$

$$IIP_3 \text{ (dBm)} \approx A_{1dB} \text{ (dBm)} + 9.65 \quad (39b)$$

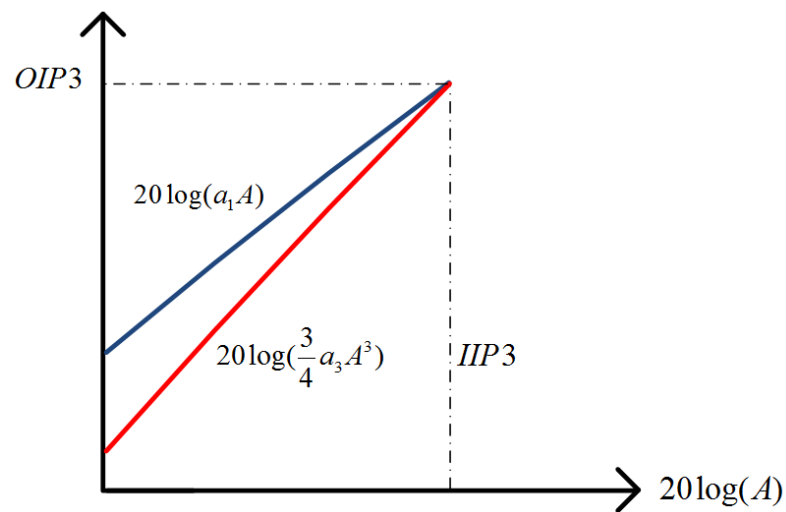


Figure 13: Third order intercept point

4.6 Noise Factor

The Noise Factor of a certain block (stage) is defined as the ratio of the input SNR to the output SNR, as shown in equation (40). This quantity is very crucial in RFIC systems design. It describes how much noise each stage is adding to the signal. Thermal noise, flicker noise and shot noise are most common sources of noise that contributes to the overall noise of a certain system block (Circuit) [17].

$$NF = \frac{SNR_{in}}{SNR_{out}} \quad (40)$$

For a cascaded system blocks the noise factor of the system can be calculated using equation (41) [18].

$$NF_{total} = NF_1 + \left(\frac{NF_2 - 1}{G_1} \right) + \left(\frac{NF_3 - 1}{G_1 G_2} \right) + \left(\frac{NF_4 - 1}{G_1 G_2 G_3} \right) + \dots \quad (41)$$

In mixer circuits, there are two definitions for noise figure; the first one is the single side band noise figure (SSB), which assumes that there is no signal at the image frequency except noise; SSB noise figure definition is useful in IF architectures. The other definition is the double side band noise figure (DSB), which assumes that the image frequency contains both image signal and noise. The DSB noise figure definition is useful in direct conversion architectures. The difference between SSB noise figure and DSB noise figure is 3 dB.

4.7 Dynamic Range

Dynamic range is defined as the ratio between the maximum signal power the receiver can detect without being driven into saturation (i.e. nonlinearity), and the minimum signal power the receiver can detect. Alternatively if (dB) values are used, it is defined as the difference between the maximum signal power and the minimum detectable signal power.

4.8 Spurious Free Dynamic Range (SFDR)

Spurious Free Dynamic Range is defined as the ratio between the signal power of interest (i.e. Fundamental Signal) to the maximum spurious power (Spur stands for any undesired harmonic distortion in the receiver output).

Chapter 5: Proposed Radar System Architecture Design and Simulation

5.1 System Level Design

The proposed radar system architecture uses similar architecture and intelligent frequency plan as in [12]. Figure 14 shows the transmitter architecture. The transmitter of the radar is fed with a chirp signal of 300 MHz instantaneous bandwidth, ranging from 200 - 500 MHz in frequency spectrum. The chirp signal is up converted and passed to a frequency doubler which doubles its center frequency and stretches its bandwidth to 600 MHz. The flat spectrum 600 MHz chirp waveform at the transmitter output provides high range resolution of 0.25 m.

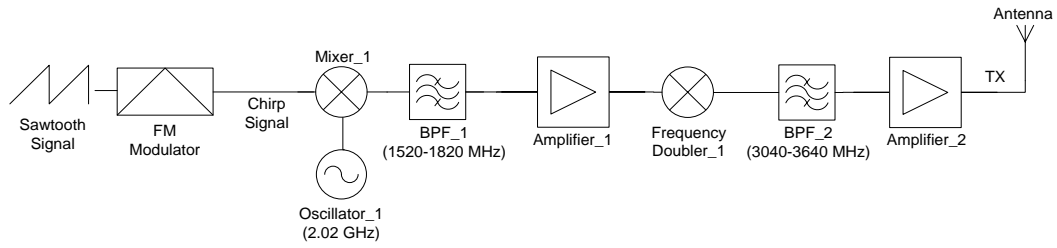


Figure 14: Block diagram of radar transmitter architecture

Figure 15 shows the local oscillator (LO) channel architecture. The LO channel functionality is identical to the transmitter, except that the LO channel chirp is up converted to a different center frequency from the transmitter chirp.

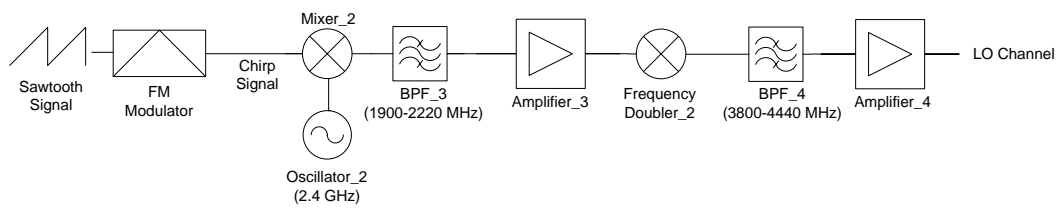


Figure 15: Block diagram of radar LO channel architecture

The architecture of the transmitter and the LO channel possesses an advantage by having a two stage up conversion that prevents spurs and intermodulation products from appearing inside the chirp band. To reduce non linearity effects a high linearity passive mixers and doublers were considered, generated spurs by each mixer and

frequency doubler are filtered using bandpass filters. Amplifiers are used to maintain adequate signal level.

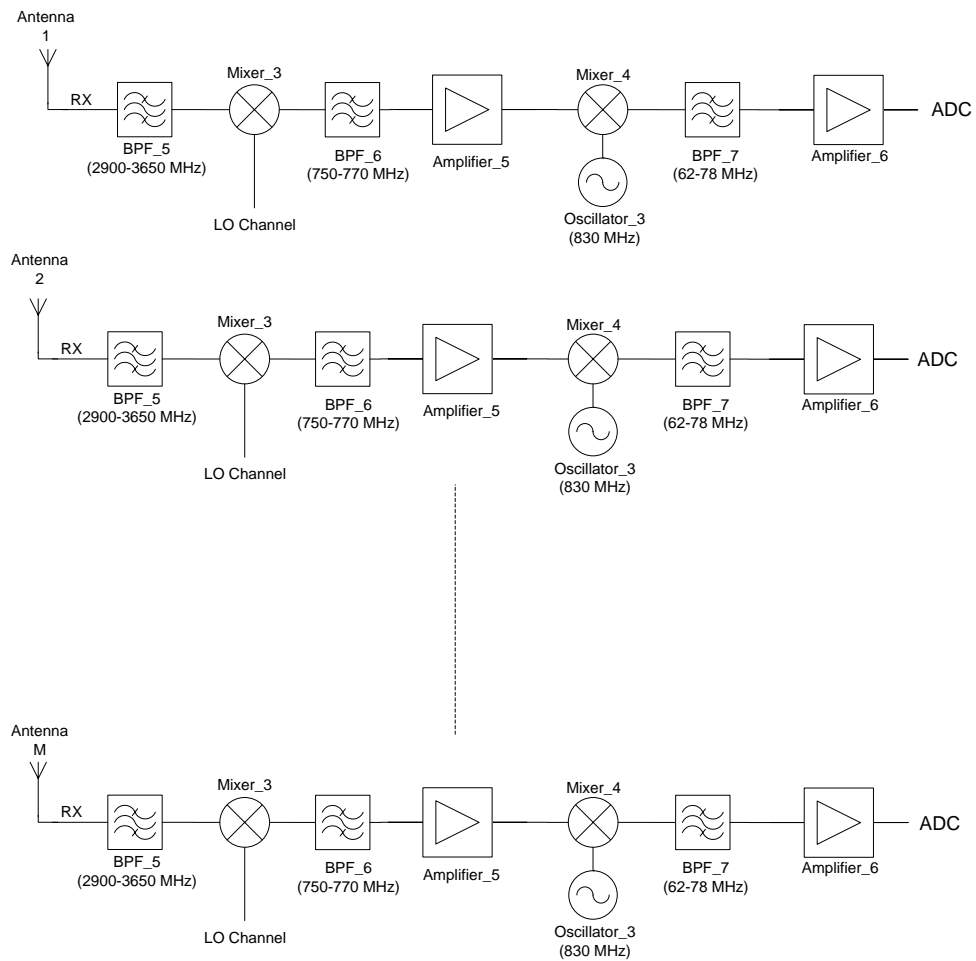


Figure 16: Block diagram of radar receiver architecture

Figure 16 shows the receiver architecture. The architecture follows a superhetrodyne architecture that down converts the signal at two stages. This not only provides immunity against the leakage of the LO channel chirp, but also reduces the effect of spurs and intermodulation products and hence maintaining high dynamic range performance. The receiver front end filter selects the received echo signal and multiplies it with the LO channel signal, then it down converts it to the intermediate frequency (70 MHz). Down converting the target signal to 70 MHz reduces analog to digital converter sampling rate requirement at the receiver side. Providing multiple receiver channels enable digital antenna beamforming and spatially mitigating interferes.

Figure 17 shows a prototype for the radar chipset system. The prototype proposes integrating the radar transmitter, local oscillator channel and receiver on a single chip. In this prototype only one receiver is shown, however, multiple replicas of the receiver can be provided to allow the implementation of digital beamforming algorithms. Filtration stages and chirp signal generator are assumed to be off chip. The dynamic range of the radar highly depends on the quality of filters (i.e. sharpness and flatness), therefore, 8th order flat and sharp Butterworth topology was considered for both transmitter and LO-Channel filters. 5th order Butterworth topology was considered for receiver filters. As on-chip inductors and capacitors have relatively lower quality factor values compared to off chip components, usually promising on chip inductors have a quality factor of 15, this will reduce the average quality factor of the whole filter and hence reduce the flatness of the filter. In section 5.2 it will be shown by the simulation results that reducing the average quality factor of the reactive elements of the filters from 100 to 20 reduces the dynamic range of the system from 60 to 41 dB. Moreover, the design of flat and sharp filters on-chip will require large area on-chip, therefore, filters are considered to be off-chip.

Detailed system level design was carried out to define the specifications of each block in the system. Tables 2 - 5 show detailed system level spread sheet design calculations.

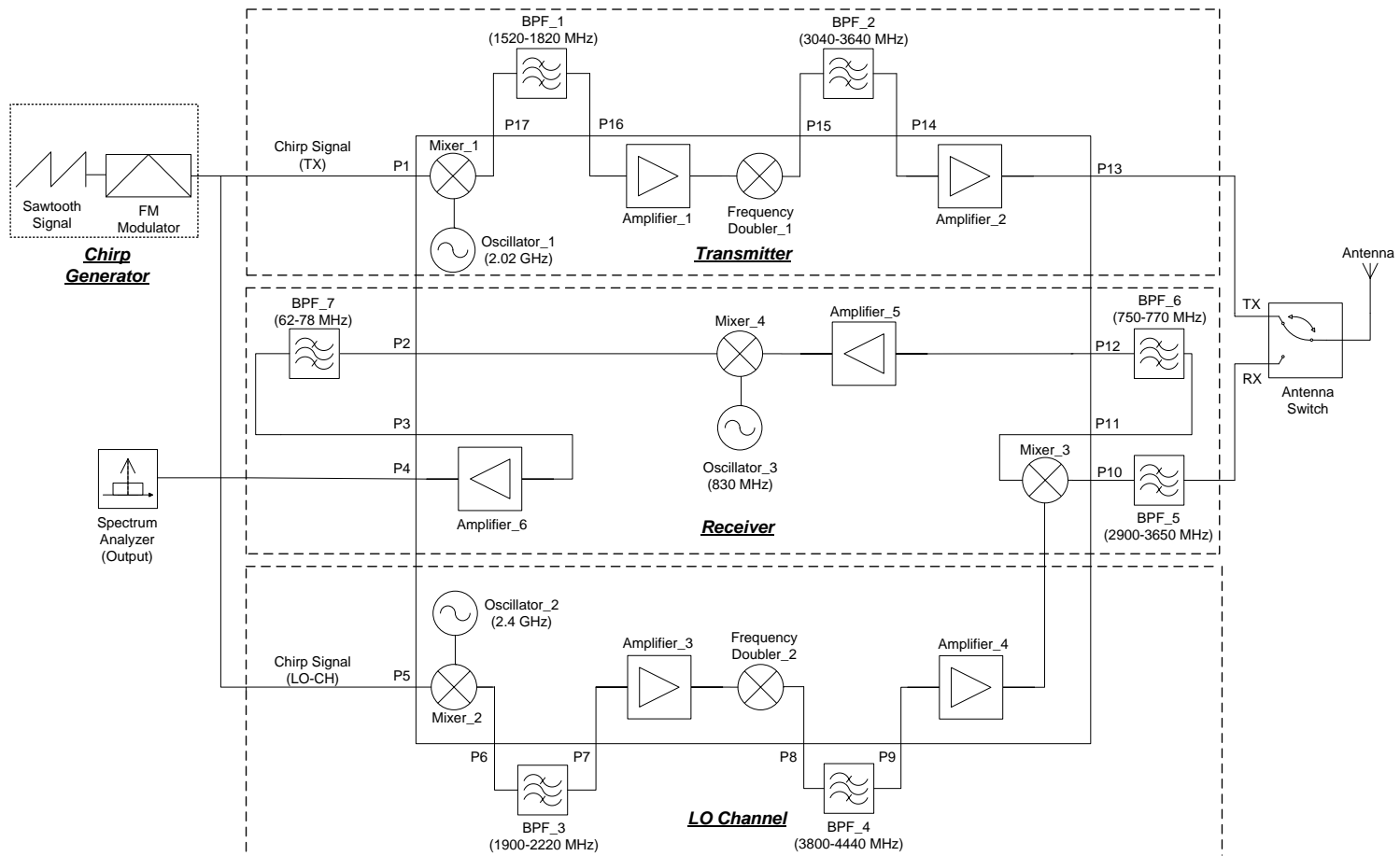


Figure 17: High level heterodyne system architecture

Table 2: Transmitter stage performance spread sheet

Stage Performance		TX							
		Pad	Mixer_1	BPF_1	Amplifier_1	Freq. Doubler_1	BPF_2	Amplifier_2	Pad
Power gain	dB	0	-8	-3	20	-12	-3	17	0
Voltage gain	linear	1	0.398107171	0.707945784	10	0.251188643	0.707945784	7.079457844	1
NF	dB	0	8	3	3	12	3	3	0
Input noise power (added)	watts	1.20E-12	6.37467E-12	1.19491E-12	1.19491E-12	1.78276E-11	1.19491E-12	1.19491E-12	0
Input noise density	V/rootHz	4.47E-10	1.03E-09	4.46E-10	4.46E-10	1.22E-09	3.16E-10	3.16E-10	0.00E+00
Input noise voltage	volts	7.7479E-06	1.78531E-05	7.72953E-06	7.72953E-06	2.9856E-05	7.72953E-06	7.72953E-06	0
Input 1dB compression	dBm	90	5	90	0	6	90	0	90
Input 1dB compression	V rms	7071.067812	0.397635364	7071.067812	0.223606798	0.446154217	7071.067812	0.223606798	7071.067812
Output 1dB compression	V rms	7071.067812	0.15830149	5005.932649	2.236067977	0.112068872	5005.932649	1.583014898	7071.067812
Input IP3	dBm	100	15	100	10	16	100	10	100
Input IP3	V rms	22360.67977	1.25743343	22360.67977	0.707106781	1.410863513	22360.67977	0.707106781	22360.67977
Input impedance	ohms	50	50	50	50	50	50	50	50
Bandwidth	Hz	3.00E+08	3.00E+08	3.00E+08	3.00E+08	6.00E+08	6.00E+08	6.00E+08	6.00E+08

Table 3: Receiver stage performance spread sheet

Stage Performance		RX							ADC
		BPF_5	Mixer_3	BPF_6	Amplifier_5	Mixer_4	BPF_7	Amplifier_6	
Power gain	dB	-3	-8	-3	10	-8	-3	11	50
Voltage gain	linear	0.707945784	0.398107171	0.707945784	3.16227766	0.398107171	0.707945784	3.548133892	
NF	dB	3	20	3	15	20	3	17	
Input noise power (added)	watts	1.19491E-12	1.18859E-10	1.19491E-12	3.67657E-11	1.18859E-10	1.19491E-12	5.89719E-11	
Input noise density	V/rootHz	2.82E-10	1.72E-08	1.73E-09	9.59E-09	1.72E-08	1.93E-09	1.36E-08	
Input noise voltage	volts	7.72953E-06	7.70907E-05	7.72953E-06	4.28752E-05	7.70907E-05	7.72953E-06	5.4301E-05	
Input 1dB compression	dBm	90	5	90	-10	-5	90	-10	
Input 1dB compression	V rms	7071.067812	0.397635364	7071.067812	0.070710678	0.125743343	7071.067812	0.070710678	
Output 1dB compression	V rms	5005.932649	0.15830149	5005.932649	0.223606798	0.050059326	5005.932649	0.250890954	
Input IP3	dBm	100	15	100	0	5	100	0	
Input IP3	V rms	22360.67977	1.25743343	22360.67977	0.223606798	0.397635364	22360.67977	0.223606798	
Input impedance	ohms	50	50	50	50	50	50	50	
Bandwidth	Hz	7.50E+08	2.00E+07	2.00E+07	2.00E+07	2.00E+07	1.60E+07	1.60E+07	

Table 4: Transmitter cascaded performance spread sheet

Cascaded Performance		TX							
		Pad	Mixer_1	BPF_1	Amplifier_1	Freq. Doubler_1	BPF_2	Amplifier_2	Pad
I/P Signal Power	dBm	-10							
O/P signal level	volts (rms)	0.070710678	0.028150428	0.019928977	0.199289768	0.050059326	0.035439289	0.250890954	0.250890954
O/P noise voltage	volts (rms)	7.7479E-06	7.7479E-06	7.7479E-06	0.000109442	2.84952E-05	2.0902E-05	0.000157769	0.000157769
C/N	dB	79.20601661	71.20601661	68.20601661	65.20601661	64.89427193	64.58592553	64.02927456	64.02927456
Cascaded Voltage Gain	linear	1	0.398107171	0.281838293	2.818382931	0.707945784	0.501187234	3.548133892	3.548133892
Cascaded Voltage Gain	dB	0	-8	-11	9	-3	-6	11	11
Cascaded I/P ref noise	volts (rms)	7.7479E-06	1.94619E-05	2.74906E-05	3.88315E-05	4.02505E-05	4.17051E-05	4.44653E-05	4.44653E-05
Cascaded NF	dB	0.00	8.00	11.00	14.00	14.31	14.62	15.18	15.18
Cascaded IIP3	volts (rms)	22360.67977	1.257433428	1.257433427	1.124148291	0.457301068	0.457301068	0.435020204	0.435020203
Cascaded IIP3	dBm	100	14.99999999	14.99999998	14.02677205	6.214344273	6.214344272	5.780488505	5.780488485
Cascaded SNR at Block Outp	dB	79.21	71.21	68.21	65.21	64.89	64.59	64.03	64.03
Receiver Output Power	dBm								
Receiver Output Noise	dBm								

Table 5: Receiver cascaded performance spread sheet

Cascaded Performance		RX							ADC
		BPF_5	Mixer_3	BPF_6	Amplifier_5	Mixer_4	BPF_7	Amplifier_6	
I/P Signal Power	dBm								
O/P signal level	volts (rms)	0.177617193	0.070710678	0.050059326	0.15830149	0.063020958	0.044615422	0.15830149	
O/P noise voltage	volts (rms)	0.000111826	5.40722E-05	3.86693E-05	0.000182582	7.89006E-05	5.61247E-05	0.000277086	
C/N	dB	64.01886273	62.33021397	62.24236398	58.7605607	58.04809534	58.00661388	55.13741072	
Cascaded Voltage Gain	linear	2.511886432	1	0.707945784	2.238721139	0.891250938	0.630957344	2.238721139	
Cascaded Voltage Gain	dB	8	-9.64327E-16	-3	7	-1	-4	7	
Cascaded I/P ref noise	volts (rms)	4.45186E-05	5.40722E-05	5.46219E-05	8.15562E-05	8.85279E-05	8.89517E-05	0.00012377	
Cascaded NF	dB	15.19	16.88	16.96	20.45	21.16	21.20	24.07	
Cascaded IIP3	volts (rms)	0.435020202	0.328359016	0.328359016	0.227634617	0.140033011	0.140033011	0.130234722	
Cascaded IIP3	dBm	5.780488464	3.337278876	3.337278875	0.155066113	-4.065091511	-4.065091511	-4.695164281	
Cascaded SNR at Block Outp	dB	64.02	62.33	62.24	58.76	58.05	58.01	55.14	
Receiver Output Power	dBm	-3							
Receiver Output Noise	dBm	-58.13741072							

After assigning the specifications of each block in the system, the cascaded performance calculations results are shown in Table 6. As the results show, the assigned specifications resulted in a total calculated dynamic range of 55.13 dB.

Table 6: Spread sheet system design main results

Dynamic range (dB)	55.13 dB
Noise Figure (dB)	24.07 dB
IIP3 (dBm)	-4.69 dBm
Cascaded voltage gain (dB)	7 dB
Power level at the ADC input (dBm)	-3 dBm

Tables 7 - 18 shows the key specifications of each block in the proposed radar chipset system in Figure 17.

Table 7: Mixer (1) Specifications

Conversion Gain (dB)	-8 dB
Double Sided Noise Figure (dB)	8 dB
Input 1-dB Compression Point (dBm)	5 dBm
Input Third Order Intercept Point (dBm)	15 dBm
LO Frequency (GHz)	2.02 GHz

Table 8: Mixer (2) Specifications

Conversion Gain (dB)	-8 dB
Double Sided Noise Figure (dB)	8 dB
Input 1-dB Compression Point (dBm)	5 dBm
Input Third Order Intercept Point (dBm)	15 dBm
LO Frequency (GHz)	2.4 GHz

Table 9: Mixer (3) Specifications

Conversion Gain (dB)	-8 dB
Double Sided Noise Figure (dB)	20 dB
Input 1-dB Compression Point (dBm)	5 dBm
Input Third Order Intercept Point (dBm)	15 dBm
LO Frequency (MHz)	(3800 - 4440) MHz

Table 10: Mixer (4) Specifications

Conversion Gain (dB)	-8 dB
Noise Figure (dB)	20 dB
Input 1-dB Compression Point (dBm)	5 dBm
Input Third Order Intercept Point (dBm)	15 dBm
LO Frequency (MHz)	830 MHz

Table 11: Frequency Doubler (1) Specifications

Conversion Gain (dB)	-12 dB
Noise Figure (dB)	12 dB
Input 1-dB Compression Point (dBm)	6 dBm
Input Third Order Intercept Point (dBm)	16 dBm
Input Frequency Range (MHz)	(1520 - 1820) MHz
Output Frequency Range (MHz)	(3040 - 3640) MHz

Table 12: Frequency Doubler (2) Specifications

Conversion Gain (dB)	-12 dB
Noise Figure (dB)	12 dB
Input 1-dB Compression Point (dBm)	6 dBm
Input Third Order Intercept Point (dBm)	16 dBm
Input Frequency Range (MHz)	(1900 - 2220) MHz
Output Frequency Range (MHz)	(3800 - 4440) MHz

Table 13: Amplifier (1) Specifications

Gain (dB)	20 dB
Noise Figure (dB)	3 dB
Input 1-dB Compression Point (dBm)	0 dBm
Input Third Order Intercept Point (dBm)	10 dBm
Frequency Range (MHz)	(1520 - 1820) MHz

Table 14: Amplifier (3) Specifications

Gain (dB)	20 dB
Noise Figure (dB)	3 dB
Input 1-dB Compression Point (dBm)	0 dBm
Input Third Order Intercept Point (dBm)	10 dBm
Frequency Range (MHz)	(1900 - 2220) MHz

Table 15: Amplifier (2) Specifications

Gain (dB)	17 dB
Noise Figure (dB)	3 dB
Input 1-dB Compression Point (dBm)	0 dBm
Input Third Order Intercept Point (dBm)	10 dBm
Frequency Range (MHz)	(3040 - 3640) MHz

Table 16: Amplifier (4) Specifications

Gain (dB)	17 dB
Noise Figure (dB)	3 dB
Input 1-dB Compression Point (dBm)	0 dBm
Input Third Order Intercept Point (dBm)	10 dBm
Frequency Range (MHz)	(3800 - 4440) MHz

Table 17: Amplifier (5) Specifications

Gain (dB)	10 dB
Noise Figure (dB)	15 dB
Input 1-dB Compression Point (dBm)	-10 dBm
Input Third Order Intercept Point (dBm)	0 dBm
Frequency Range (MHz)	(750 - 770) MHz

Table 18: Amplifier (6) Specifications

Gain (dB)	11 dB
Noise Figure (dB)	17 dB
Input 1-dB Compression Point (dBm)	-10 dBm
Input Third Order Intercept Point (dBm)	0 dBm
Frequency Range (MHz)	(62 - 78) MHz

5.2 System Level Simulation

The radar system level performance was simulated using AWR Design Environment visual system simulator (VSS). Figures 18 - 30 show simulation results.

Figure 18 shows the spectrum of the input chirp to both transmitter and local oscillator channel, the spectrum of the chirp is confined between 0.2 GHz and 0.5 GHz (300 MHz instantaneous bandwidth). Figure 19 shows the instantaneous frequency of the input chirp with respect to time, and shows that the frequency increases linearly from 0.2 GHz to 0.5 GHz within 100 μ sec.

The transmitter up converts the input chirp and doubles its bandwidth. Figure 20 shows the output spectrum of the transmitter. The transmitter output chirp is confined between 3.04 GHz and 3.64 GHz (600 MHz instantaneous bandwidth). Figure 21 shows the instantaneous frequency of the transmitter output chirp with respect to time.

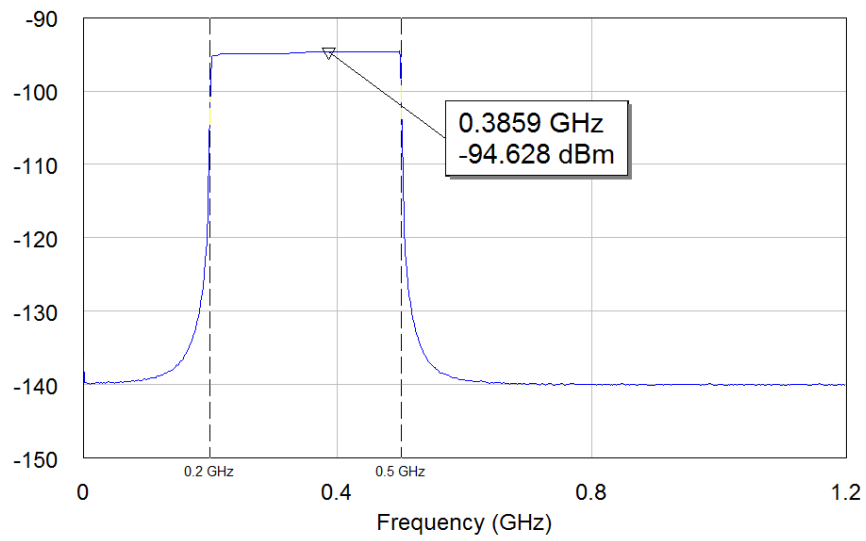


Figure 18: Input chirp signal (dBm), 300 MHz instantaneous bandwidth

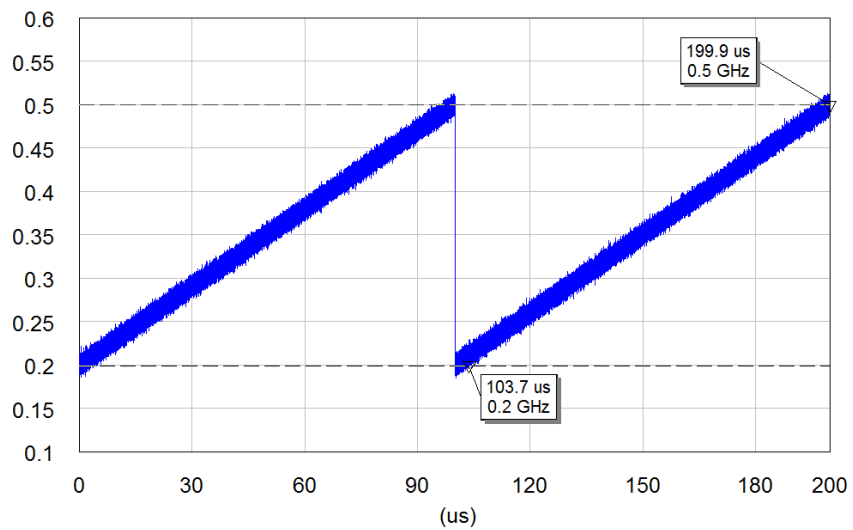


Figure 19: Chirp signal instantaneous frequency (GHz)

Figure 22 shows the local oscillator (LO) channel chirp output spectrum. The LO channel chirp spectrum is confined between 3.8 GHz and 4.4 GHz (instantaneous frequency of 600 MHz). Figure 23 shows the LO channel chirp instantaneous frequency with respect to time.

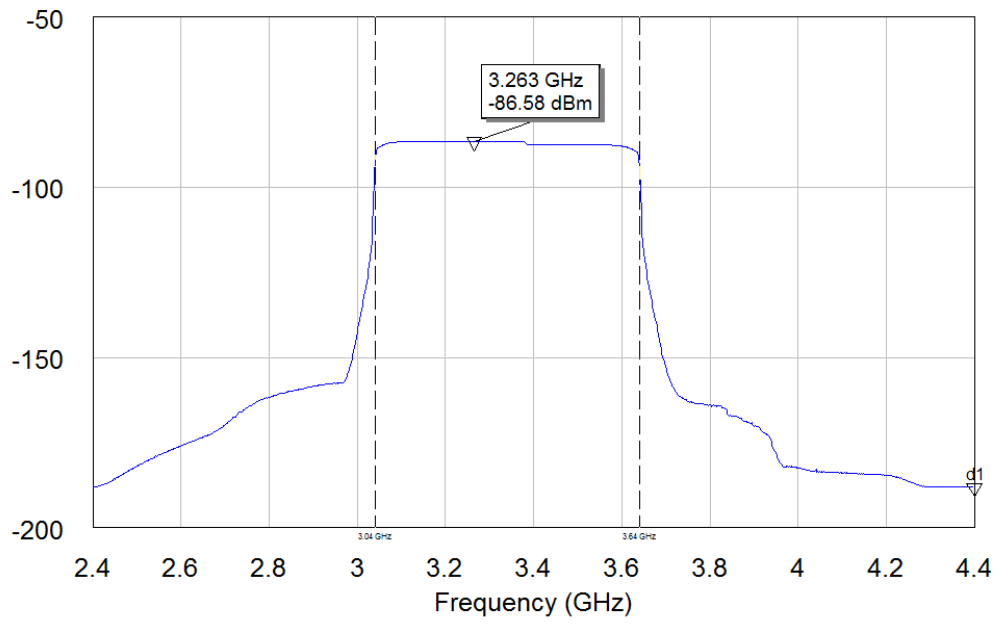


Figure 20: Radar transmitter output spectrum (dBm)

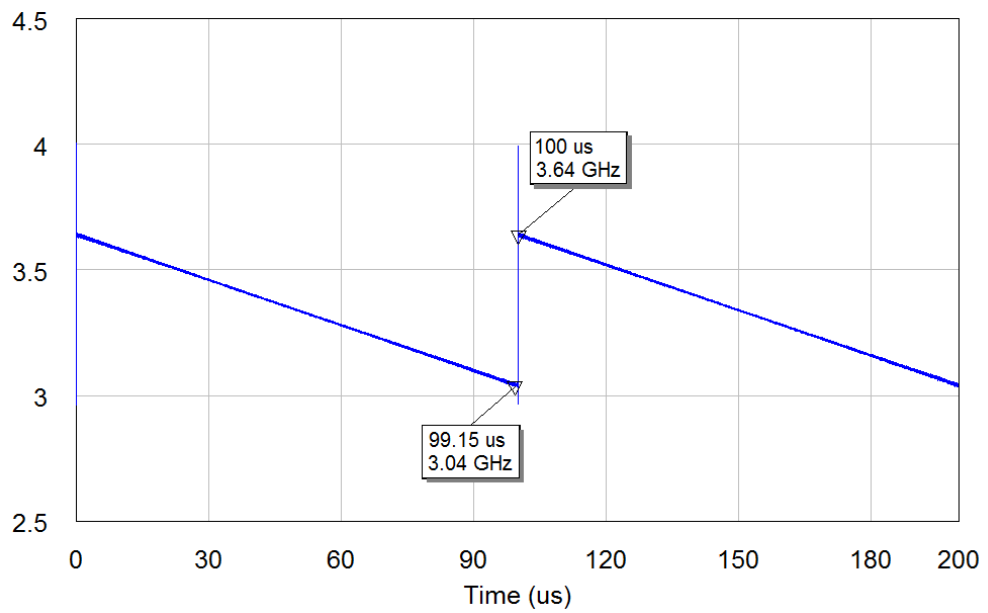


Figure 21: Transmitter output chirp instantaneous frequency (GHz)

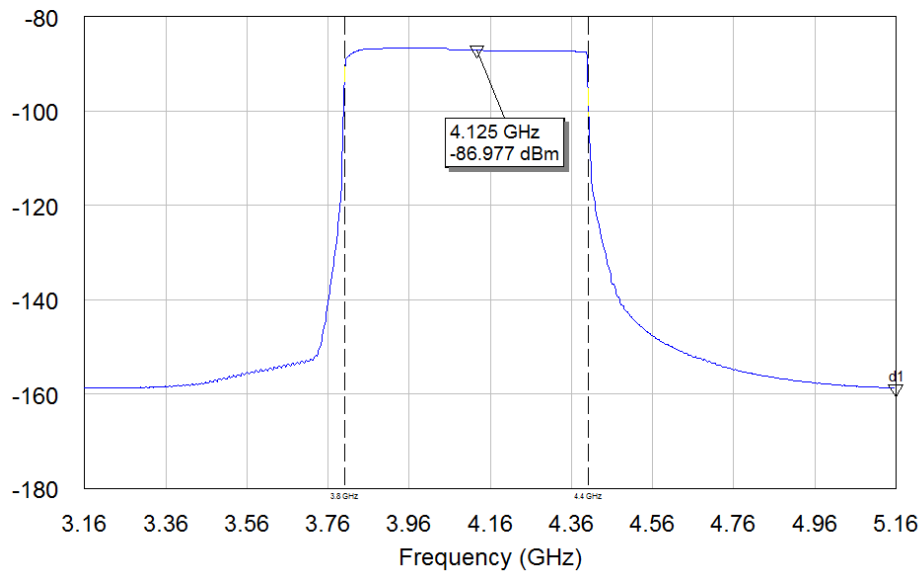


Figure 22: Radar LO channel output spectrum (dBm)

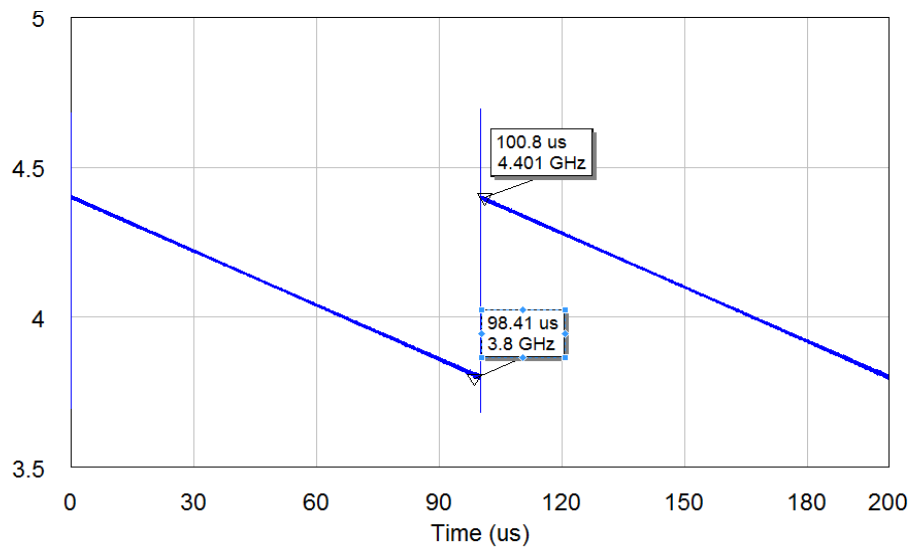


Figure 23: LO channel output chirp instantaneous frequency (GHz)

Figure 24 shows the receiver output spectrum. The transmitter signal was mixed with the local oscillator channel signal and down converted to the intermediate frequency. The receiver output spectrum shows a single tone centered at 70 MHz. In-band dynamic range is 60 dB which is considered to be good. Also, Figure 25 shows the time domain output of the receiver.

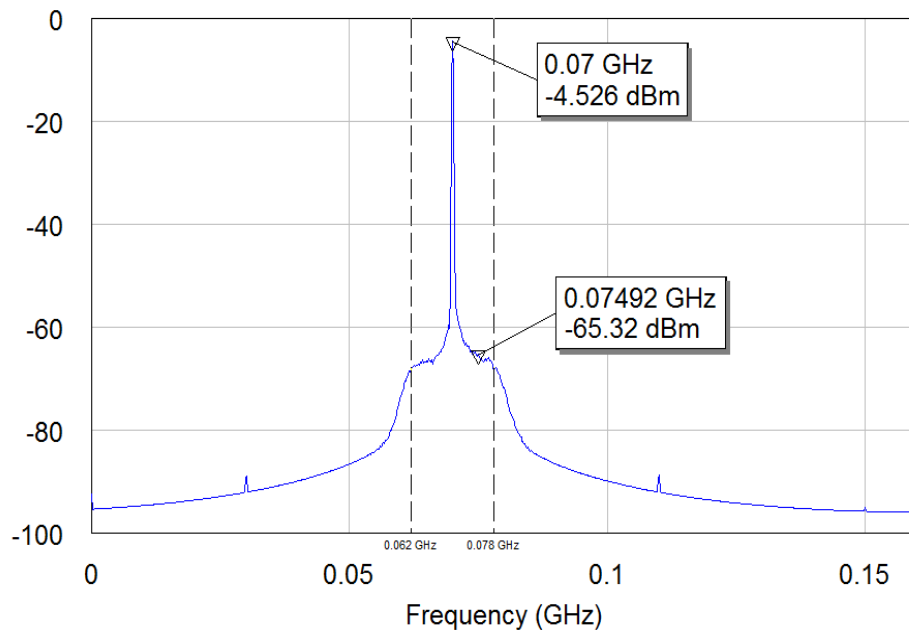


Figure 24: Receiver output spectrum (dBm)

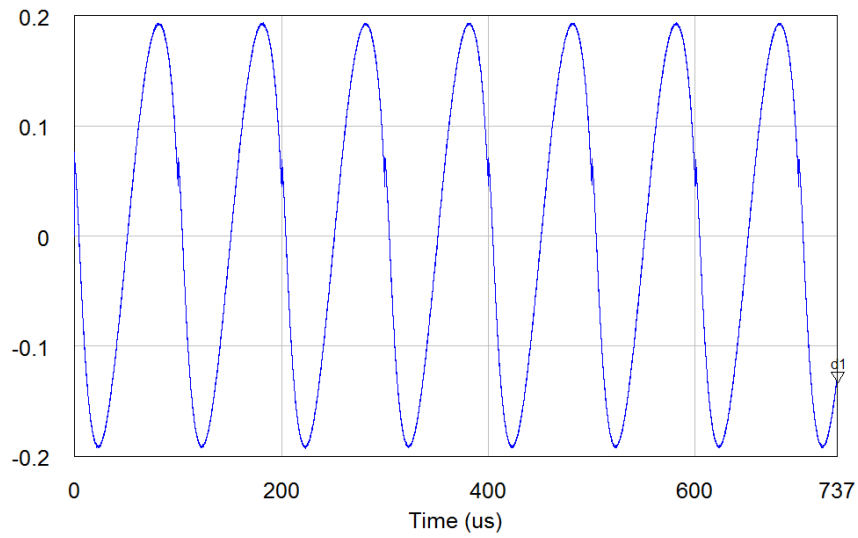


Figure 25: Receiver time domain output (V)

Figure 26 shows the instantaneous frequency of the receiver output with respect to time (constant at 70 MHz).

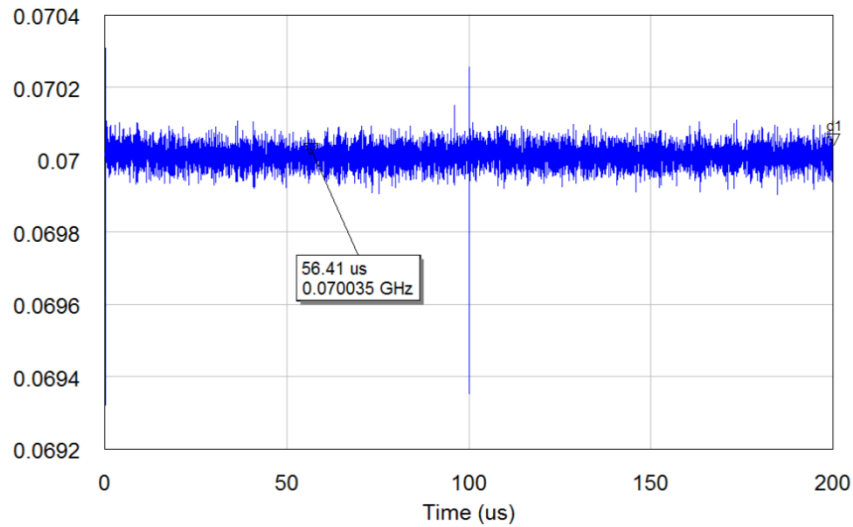


Figure 26: Receiver output instantaneous frequency (GHz) vs time

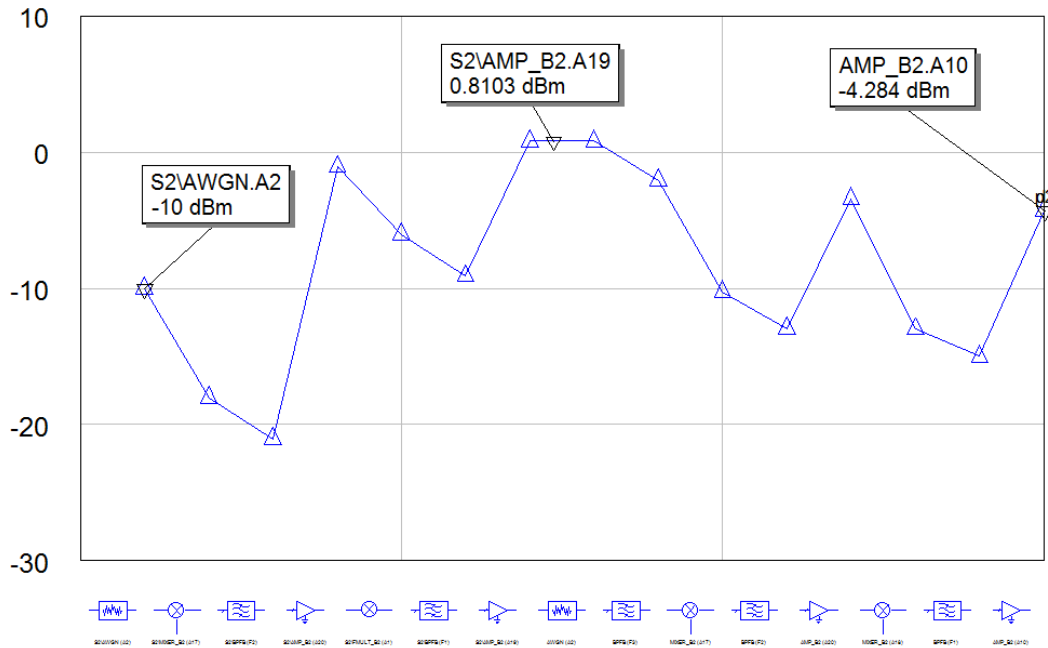


Figure 27: Cascaded signal power level from transmitter input to receiver output (dBm)

Figure 27 shows the cascaded signal power level at each stage, an input of -10 dBm results in an output of -4.284 dBm (total gain of 5.716 dB).

As an example, Figure 28 shows BPF (2) frequency response when the average quality factor of reactive elements is 100, while Figure 29 shows the frequency response of the same filter when the average quality factor of reactive

elements is 20. As obvious from the two figures the flatness of the filter decreases dramatically by decreasing the average quality factor of reactive elements, moreover, the losses of the filter increase.

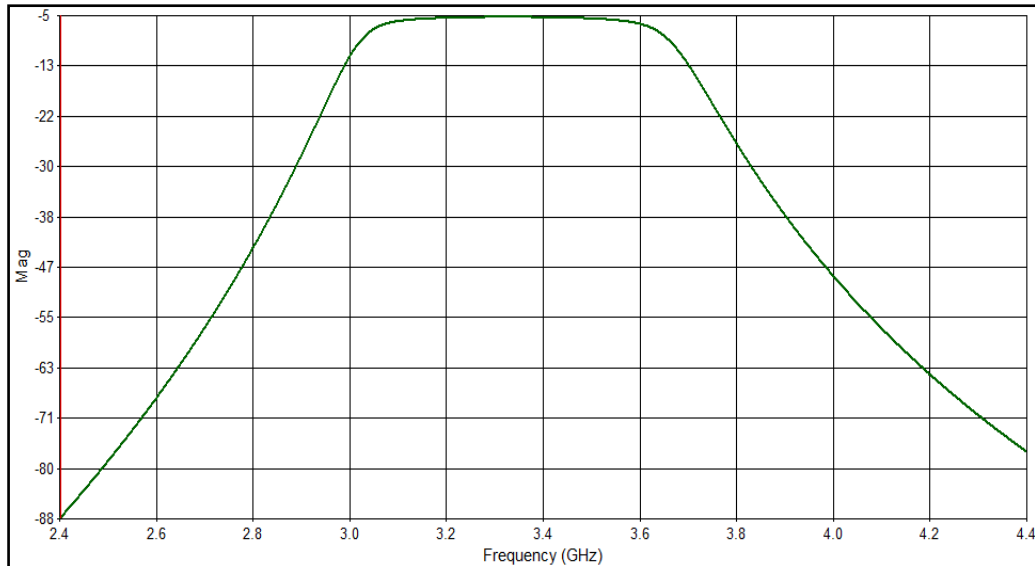


Figure 28: BPF (2) Frequency Response in dB (Reactive Elements Average Quality Factor = 100)

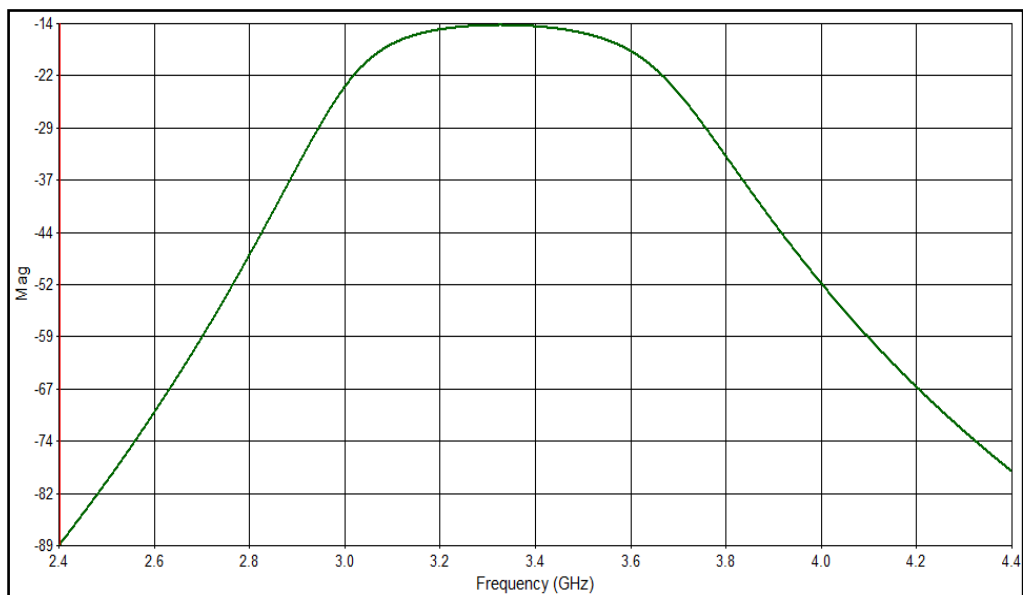


Figure 29: BPF (2) Frequency Response in dB (Reactive Elements Average Quality Factor = 20)

Figure 30 shows the receiver output when using filters with reactive elements average quality factor of 20, as it shows the dynamic range is reduced to 41 dB.

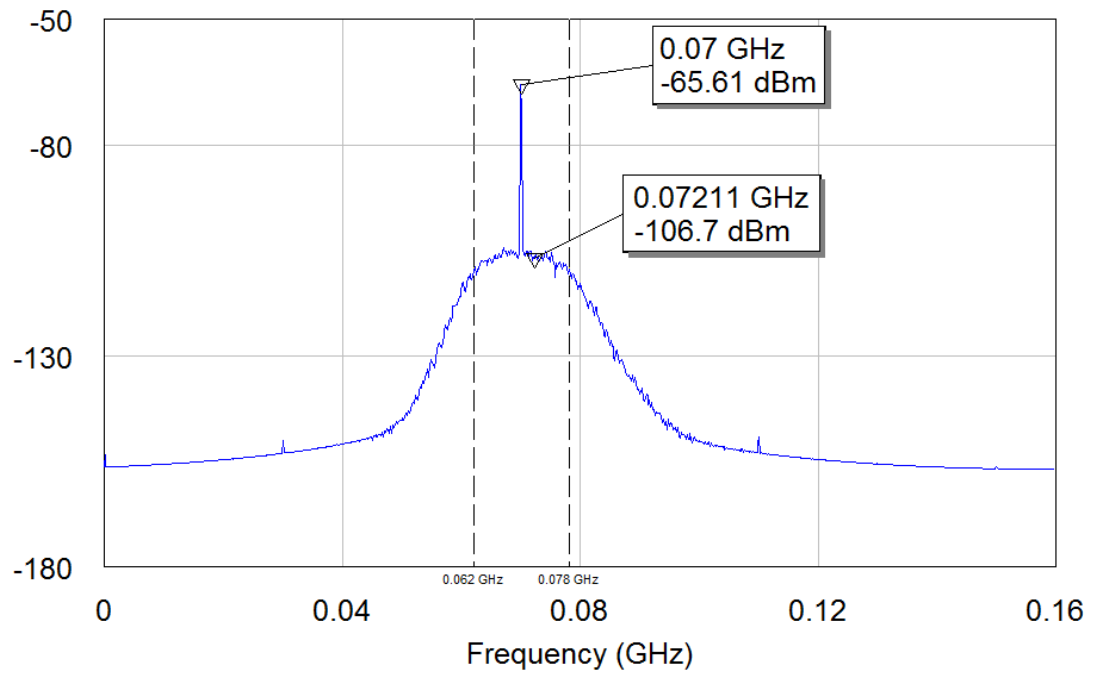


Figure 30: Receiver Output Using Filters with Reactive Elements Average Quality Factor of 20

Chapter 6: Circuit Level Design and Simulation

6.1 Introduction

The circuit level design is focused on designing the receiver blocks. Figure 31 shows the receiver system blocks. The filters shown in the receiver system block diagram are 5th order off chip Butterworth filters as per the system design provided in Chapter 5.

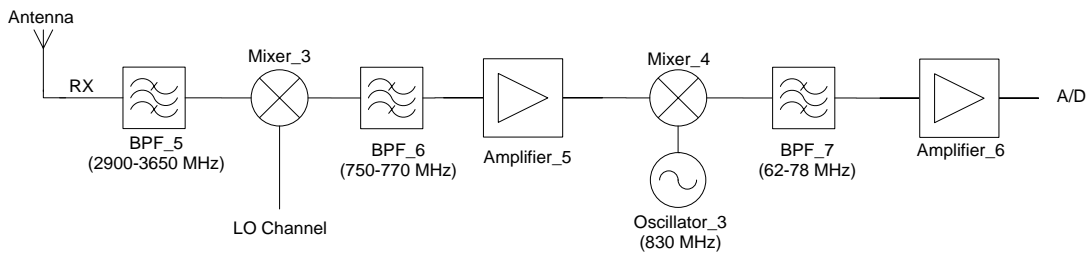


Figure 31: Receiver System Block Diagram

The following circuits were designed based on the specifications provided in Chapter 5. A 5 volts biasing voltage was chosen for all active circuits to provide a good headroom:

- Mixers (Mixer 3 and Mixer 4):

Quad passive mixer topology is considered. Also, the same mixer topology can be used for the up conversion mixers and doublers in the transmitter and the LO-Channel systems.

- First IF amplifier centered at 760 MHz (Amplifier 5):

Cascode configuration with source follower buffer stage is considered for this stage.

- Second IF amplifier centered at 70 MHz (Amplifier 6):

Common source amplifier with active load topology along with a source follower buffer stage is considered for this stage.

- Voltage controlled oscillator (Oscillator 3 operating at 830 MHz):

Negative gm cross coupled voltage controlled oscillator design is considered for this block.

6.2 Quad Passive Mixer Circuit

The main function of a mixer is to provide frequency shift in the signal spectrum. It can be an up-conversion mixer that up converts low frequency signals to a higher frequency, or a down-conversion mixer that down converts a high frequency signal to a lower frequency. There is a variety of mixer circuit topologies. Mixers are usually classified as either passive or active. Passive mixers are well known for their high linearity, while active mixers provide signal gain. Most of the time, choosing the appropriate mixer topology depends to some extent on whether linearity or gain is of more concern. This section provides a brief overview of quad passive mixer topology. Figure 32 shows a simplified quad mixer schematic. The quad mixer can provide high linearity along with high insulation levels from local oscillator to output [19].

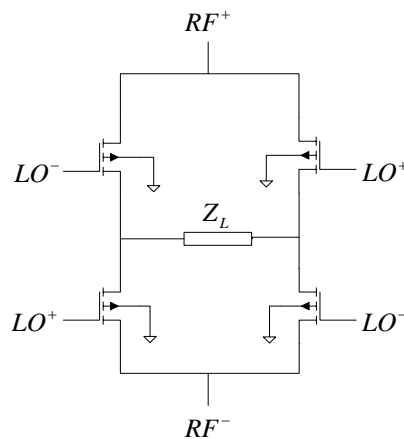


Figure 32: Quad passive mixer circuit

Quad passive mixer can be perceived as a switching circuit that reverses the current direction (i.e. voltage polarity) of the output at the same rate of the local oscillator. This operation is equivalent to multiplying the input signal with +1 and -1

square function. when evaluating the Fourier series expansion of the output, it becomes obvious that the signal is shifted in frequency domain at odd integer multiple of the local oscillator frequency. Therefore, a filtration stage after the mixer is usually provided to get rid of higher frequency spectrum replicas.

To grasp the idea of operation of a switching mixer, Figure 33 shows the equivalent circuit for a single transistor switching scenario which includes the effect of a parallel transistor in cut off state, where the gate of the transistor is connected to the local oscillator (LO). Whenever the gate voltage is high the transistor goes into the deep triode region and behaves like an almost linear resistor R_{on} . Whenever the gate voltage is low, the transistor is in the cut off region and no current passes through, and it exhibits a very high capacitive impedance Z_{off} . This switching process controlled by the local oscillator is equivalent to multiplying the signal by the square wave function $V_{LO}(t)$ as shown in Figure 33. Equation (43) shows the Fourier series expansion of $V_{LO}(t)$, from which it can be observed that there is a loss of $(1/\pi)$ for the fundamental harmonic component. In addition to the loss obtained from the switching, there is another loss due to the voltage division between Z_L and R_{on} . Equation (44) shows the total conversion loss of the mixer.

To have a high linearity mixer, R_{on} should be as linear as possible, which means that a relatively high voltage at the gate should be maintained to drive the transistor into the deep triode region. Also, to minimize the conversion loss, R_{on} should be as small as possible.

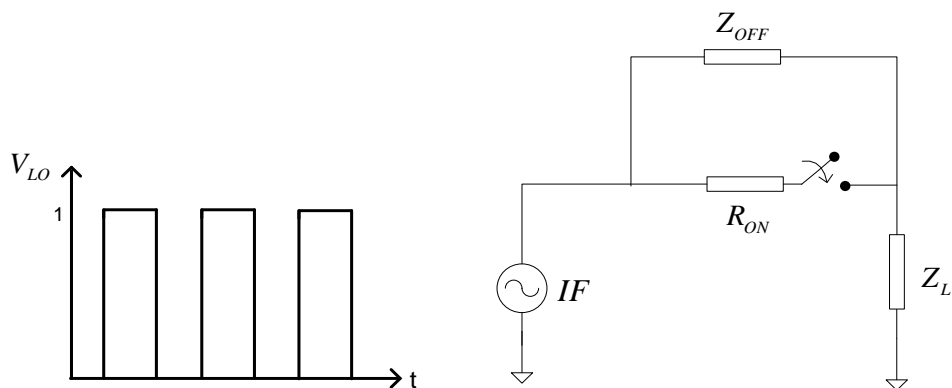


Figure 33: Equivalent circuit of a single transistor switching scenario

$$V_{out}(t) = \left(\frac{Z_L}{Z_L + R_{ON} \parallel Z_{OFF}} \right) \cdot V_{LO}(t) \cdot V_{IF}(t) \quad (42)$$

$$V_{LO}(t) = \frac{1}{2} + \frac{2}{\pi} \left[\sin(\omega_{LO}t) + \frac{\sin(3\omega_{LO}t)}{3} + \frac{\sin(5\omega_{LO}t)}{5} + \dots \right] \quad (43)$$

$$L_c = \frac{1}{\pi} \left(\frac{Z_L}{Z_L + R_{ON} \parallel Z_{OFF}} \right) \quad (44)$$

The quad passive mixer has a good advantage in terms of the input/output impedance fidelity. The input of the mixer sees the output impedance as its input and vice versa. In this way an easy matching can be achieved and the need for an extra matching network is eliminated [20].

Figure 34 shows the circuit design of a quad passive mixer. The same topology is used for both Mixer 3 and Mixer 4 in the system level diagram. Choosing passive mixer topology has the following advantages:

1. High linearity with a 1-dB compression point up to 13 dBm.
2. Transparent matching between the input and output, which eliminates the need for wide band matching networks.
3. Only four transistors are required.
4. Double balance operation which minimizes the LO leakage.
5. Passive (i.e. no power consumption).

The main disadvantage of the passive topology is its signal loss. Therefore, an amplification stage is provided after the mixer stage.

Two comparators are provided at the LO input. They transform sinusoidal waves to rectangular waves which improves both the noise and linearity performance of the mixer.

The mixer circuit was used for mixer 3 which will multiply the received wideband 600 MHz chirp from the transmitter with the LO channel chirp. Also, the same structure is used for mixer 4 to down convert the narrow band signal from 760 MHz to 70 MHz.

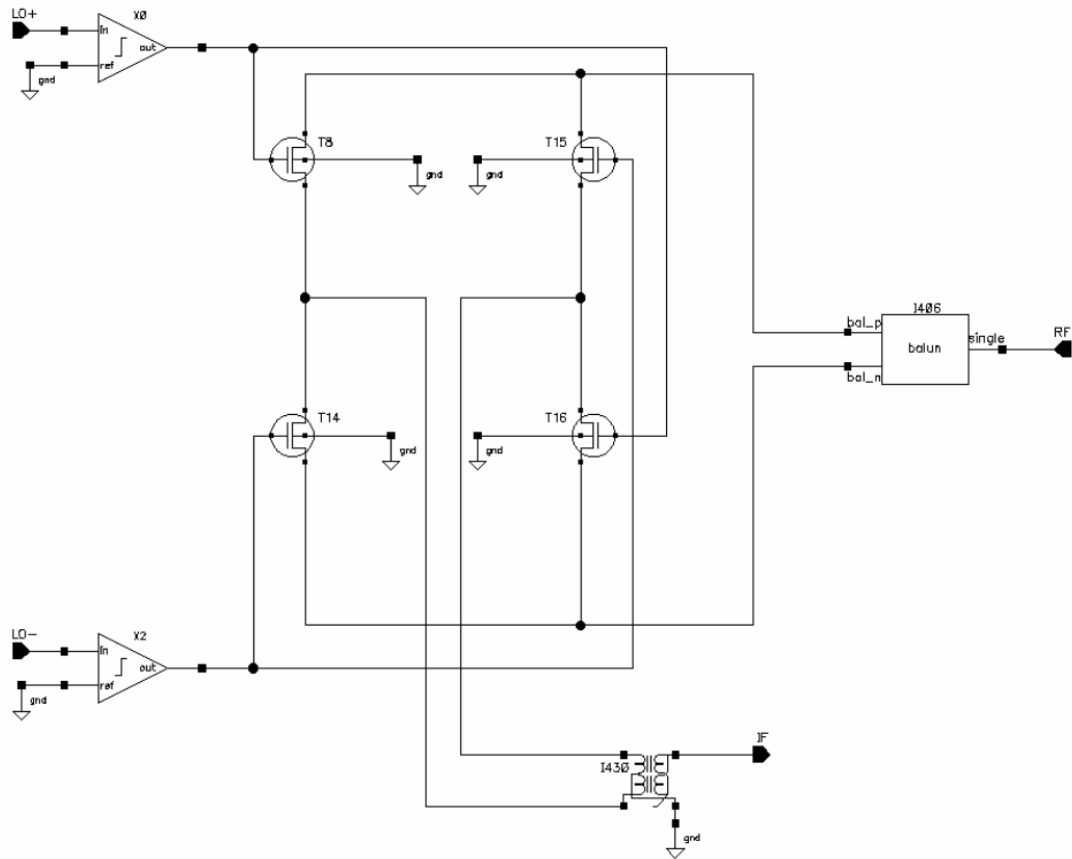


Figure 34: Quad Passive Mixer

Figure 35 shows the spectrum of the input and output of mixer 4; the input consists of two tones at both 750 MHz and 770 MHz, and the output is the down converted version to 80 MHz and 60 MHz respectively.

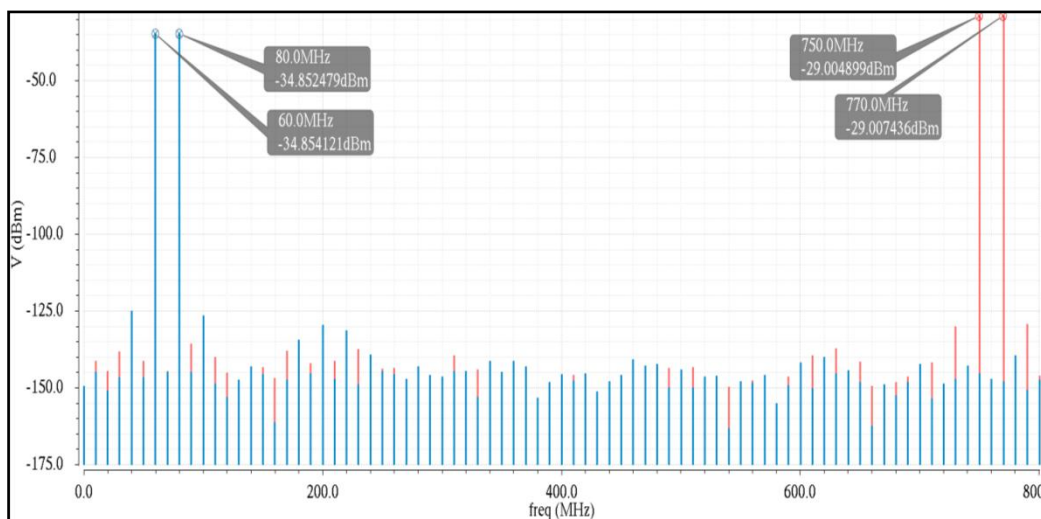


Figure 35: Input (Red) and Output (Blue) Spectrum of Mixer Circuit

Figure 36 shows the input and output S-parameters values, both S11 and S22 values are almost -17 dB over the input and output frequency range, which is considered as a good match.

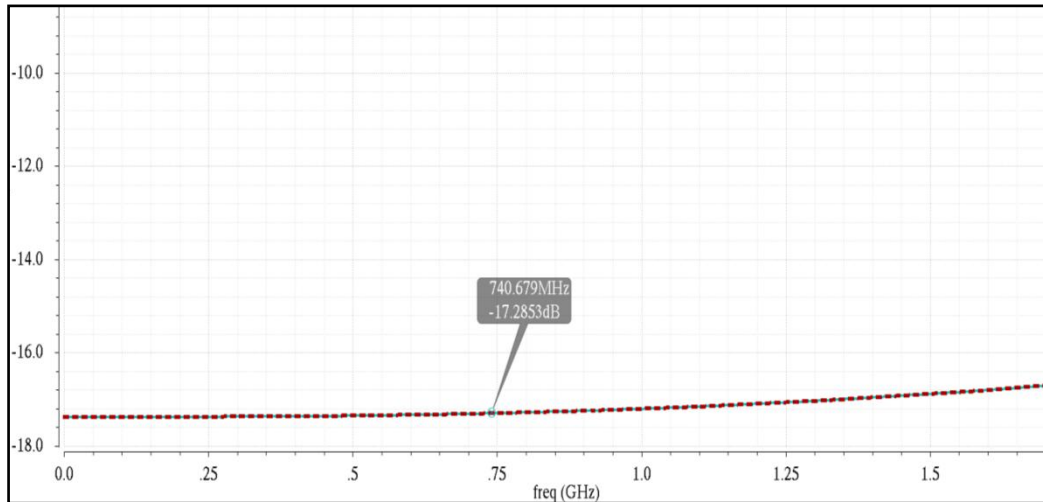


Figure 36: Mixer Circuit S11 (Red) and S22 (Cyan) in dB

Figure 37 shows the 1-dB compression point curve, the input 1-dB compression point is 14.287 dBm, which is a good linearity performance.

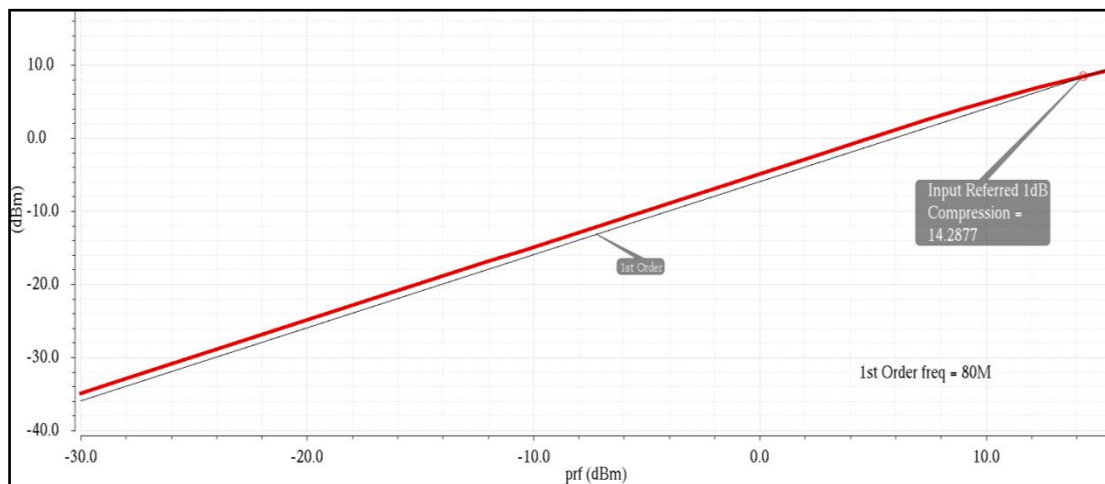


Figure 37: Mixer Circuit 1-dB Compression point

Figure 38 shows the conversion loss of the mixer circuit, a passive loss of 4.85 dB is achieved. Also, the conversion loss curve confirms a 14.287 dBm input 1-dB compression point.

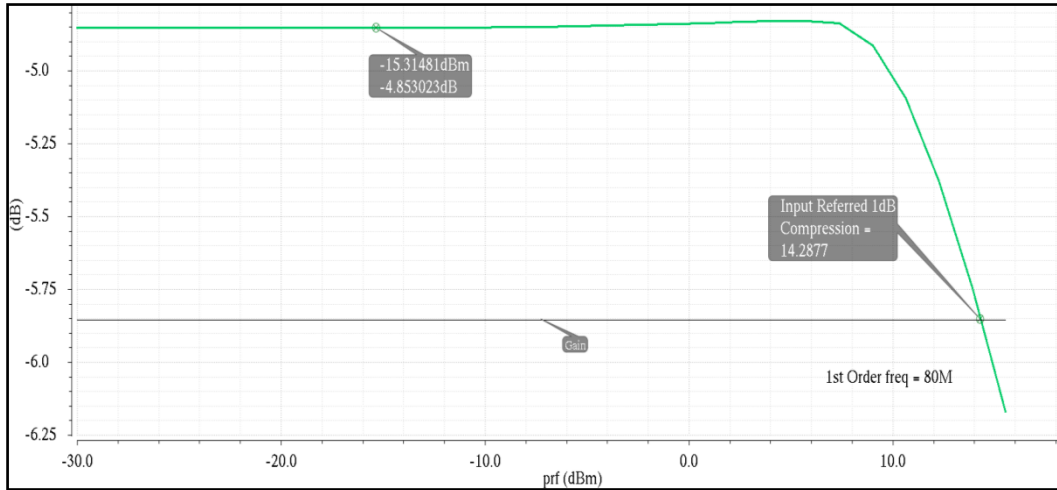


Figure 38: Mixer Circuit Conversion Gain

Figure 39 shows both single side band and double side band noise figures, the DSB NF (red) is 4.43 dB and the SSB NF (green) is 7.44 dB. As obvious, the difference is 3 dB and complying with the expected theoretical difference between DSB and SSB NF.

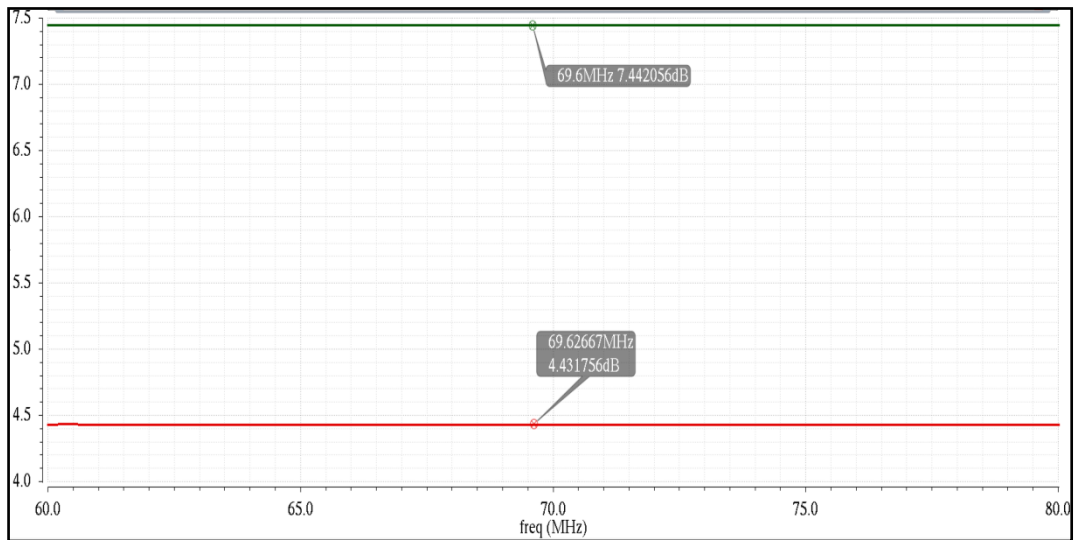


Figure 39: SSB (Green) and DSB (Red) Mixer Circuit NF in dB

The next step was to test the mixer circuit at higher frequencies and wider band. Figure 40 shows the spectrum of the input and output of mixer 3. The input consists of two tones at 3.64 GHz and 3.04 GHz, and the output is the down converted version at 760 MHz and 160 MHz respectively.

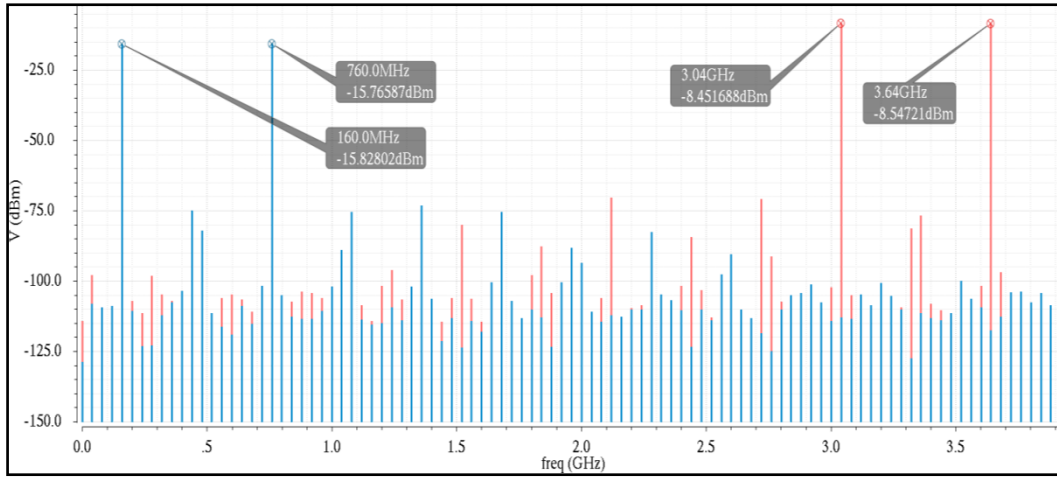


Figure 40: Input (Red) and Output (Blue) Spectrums of Mixer Circuit "Higher Frequency Test"

Figure 41 shows the conversion loss of the mixer which is about 5.75 dB, and also shows a high linearity performance with a compression point of 13.565 dBm.

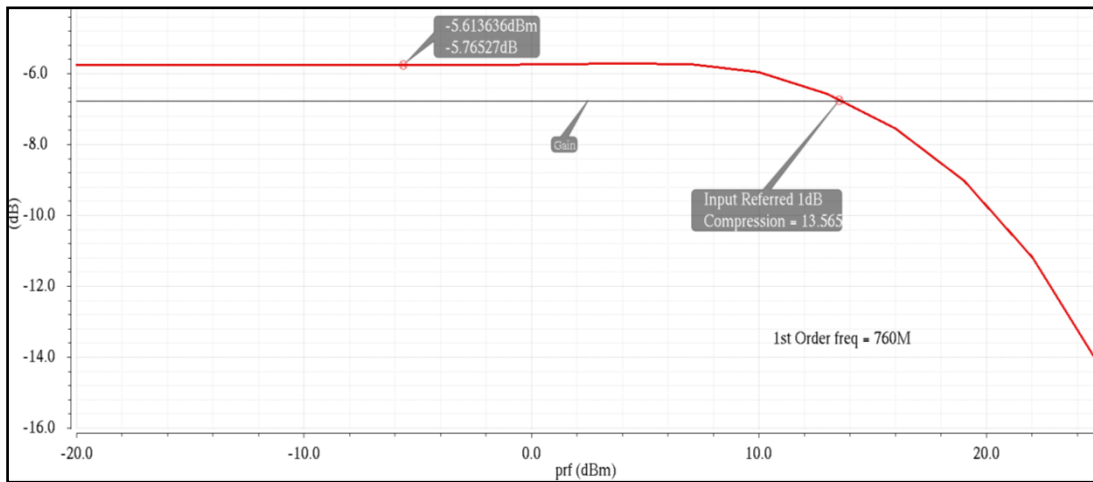


Figure 41: Conversion Loss of Mixer Circuit "Higher Frequency Test"

Figure 42 shows both input and output S-parameters of the mixer circuit. S11 and S22 values are almost -13.7 dB which is considered as a good match. As it is shown, the matching performance was degraded at higher frequency comparing to the lower frequencies, and this is due to the inclusion of the parasitic capacitances of the transistor which tend to have more effect at higher frequencies.

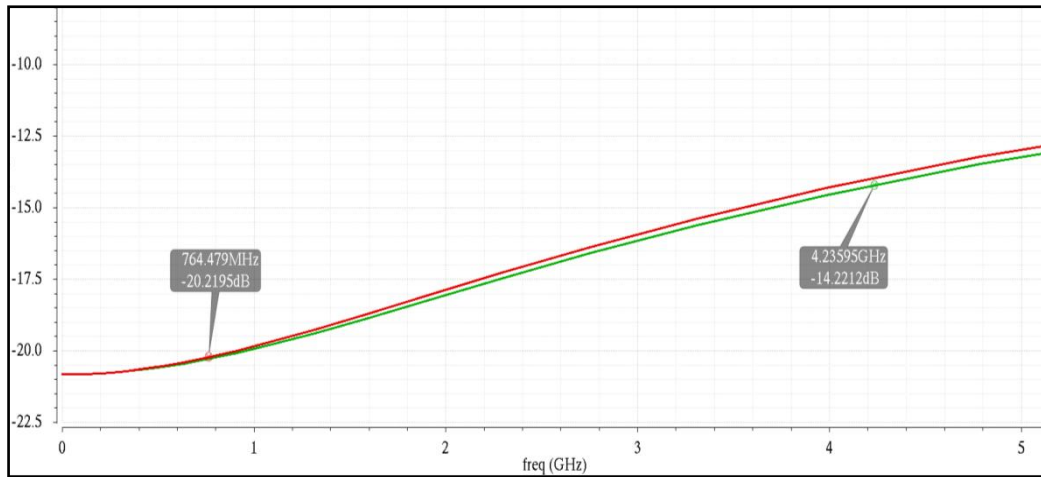


Figure 42: Mixer Circuit S11 (Red) and S22 (Green) in dB "Higher Frequency Test"

Figure 43 shows the SSB and DSB noise figure, an 8.86 dB SSB NF and 5.85 DSB NF is shown from the simulation.

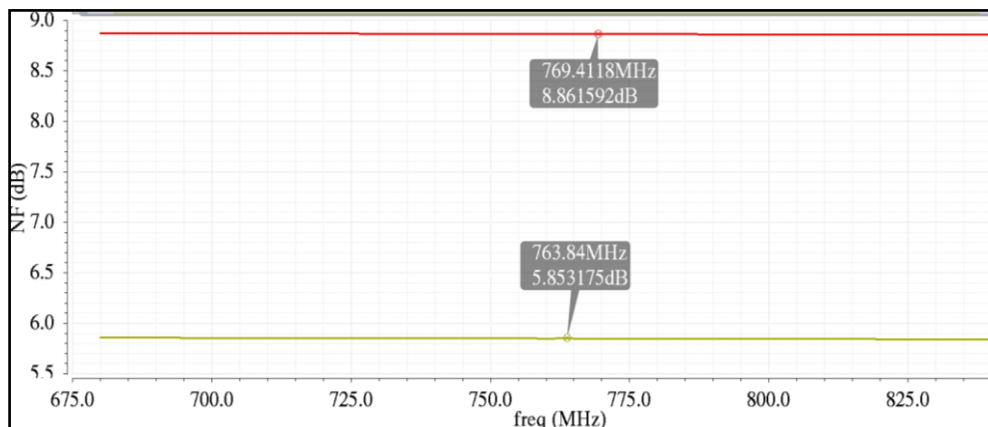


Figure 43: SSB NF (Red) and DSB NF (Yellow) of the Mixer in dB "Higher Frequency Test"

To get a more realistic simulation of the performance of the first stage mixer (mixer 3), a chirp was generated with a VCO and a sawtooth input using cadence functional blocks. The first chirp represents the received chirp from the transmitter which ranges from 3.04 GHz to 3.64 GHz as shown in (red) Figure 44. The second chirp represents the LO Channel chirp (Blue) which ranges from 3.8 GHz to 4.4 GHz as shown in (blue) Figure 44 as well.

The output spectrum of the mixer is shown in Figure 45. It shows the result of multiplying the received chirp with the LO Channel chirp. The output is a single tone

centered at 760 MHz as expected. The mixer output shows a very high output dynamic range of an almost 65 dB.

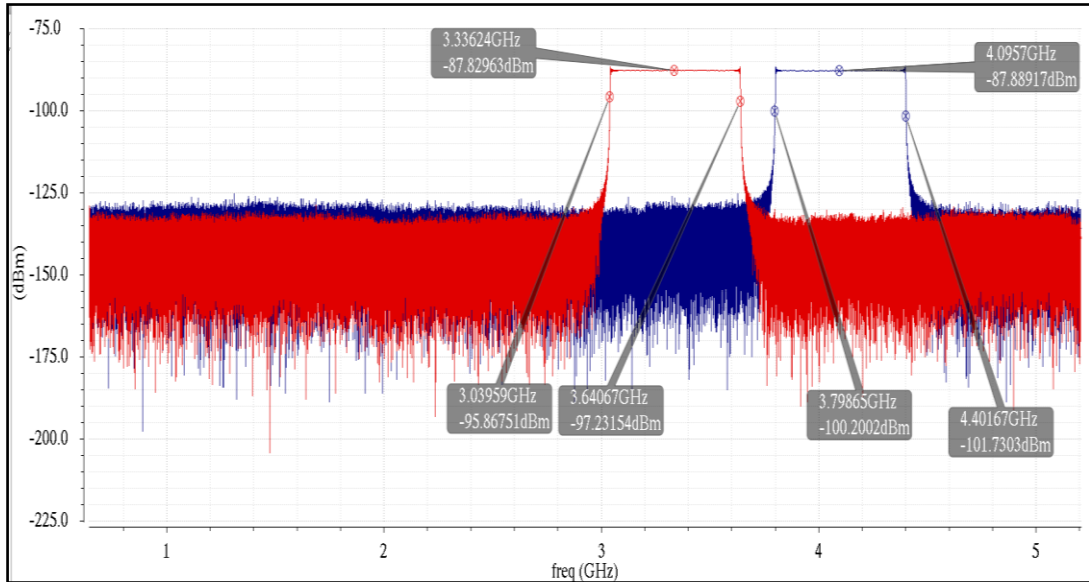


Figure 44: TX (Red) and LO Channel (Blue) Chirp Signals

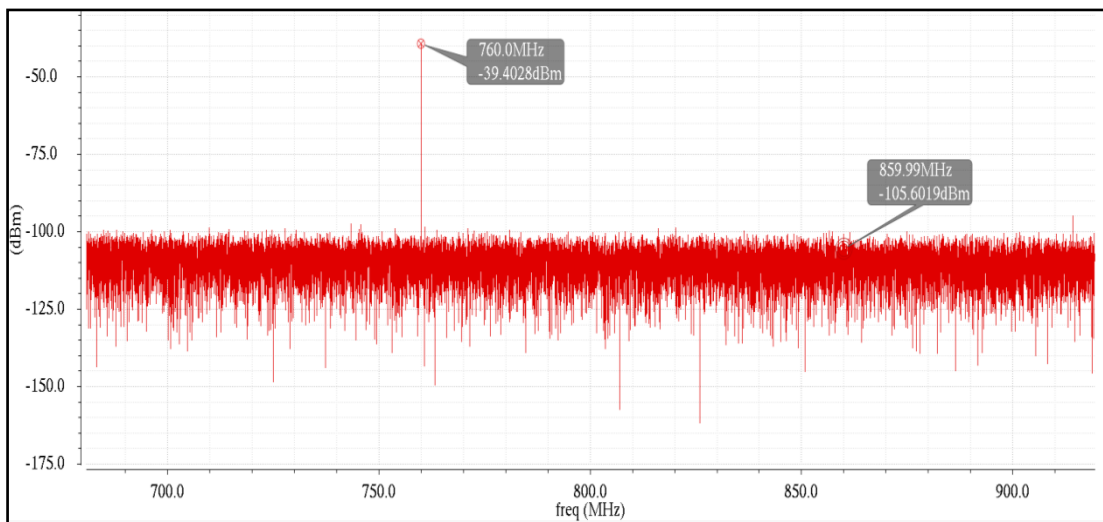


Figure 45: Mixer Output Spectrum "Chirp Input Test"

Table 19: Mixer (3) Comparison Between Achieved and Required Specs

Parameter	Required Specs	Achieved Specs
Conversion Gain (dB)	-8 dB	-5.76 dB
Double Sided Noise Figure (dB)	20 dB	5.85 dB
Input 1-dB Compression Point (dBm)	5 dBm	13.565 dBm
LO - Frequency Range	(3800 - 4440) MHz	
RF Input Frequency Range	(2900 - 3650) MHz	
IF Output Frequency Range	(750 - 770) MHz	

Table 20: Mixer (4) Comparison Between Achieved and Required Specs

Parameter	Required Specs	Achieved Specs
Conversion Gain (dB)	-8 dB	-4.85 dB
Double Sided Noise Figure (dB)	20 dB	4.431 dB
Input 1-dB Compression Point (dBm)	5 dBm	14.287 dBm
LO - Frequency (MHz)	830 MHz	
RF Input Frequency Range	(750 - 770) MHz	
IF Output Frequency Range	(62 - 78) MHz	

A figure of merit was calculated for the mixer circuit according to equation (45) [21], the obtained figure of merit value is 1 dBm / Hz.

$$FOM_{Mixer}(dBm/Hz) = G_c - SSB\ NF + P_{1-dB} - P_{Consumed} \quad (45)$$

6.3 Frequency Doubler Circuit

The same quad passive mixer design provided in section 6.2 can be used to perform frequency doubling operation, by connecting the input signal to both IF and LO ports of the mixer circuit. The output signal will be the doubled frequency version of the input signal.

Figure 47 shows the input and output spectrums of the frequency doubler; an input chirp with an instantaneous bandwidth of 300 MHz centered at 1.67 GHz is

doubled at the output to provide a chirp with 600 MHz bandwidth centered at 3.34 GHz.

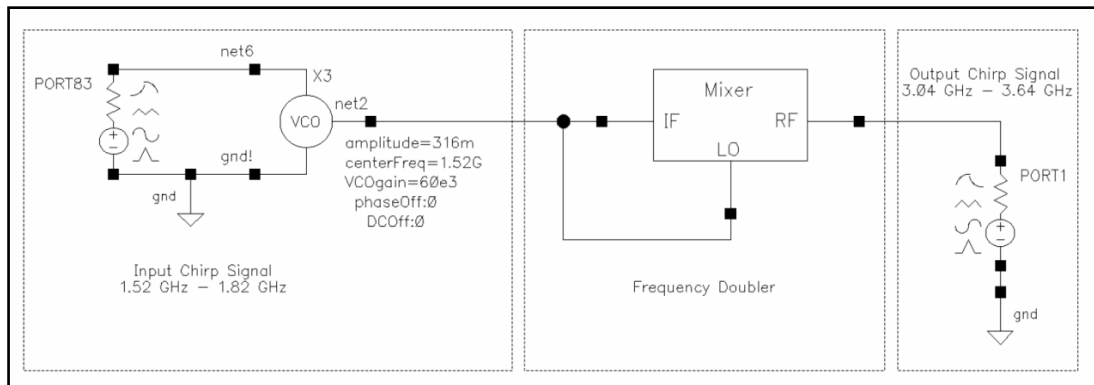


Figure 46: Frequency Doubler

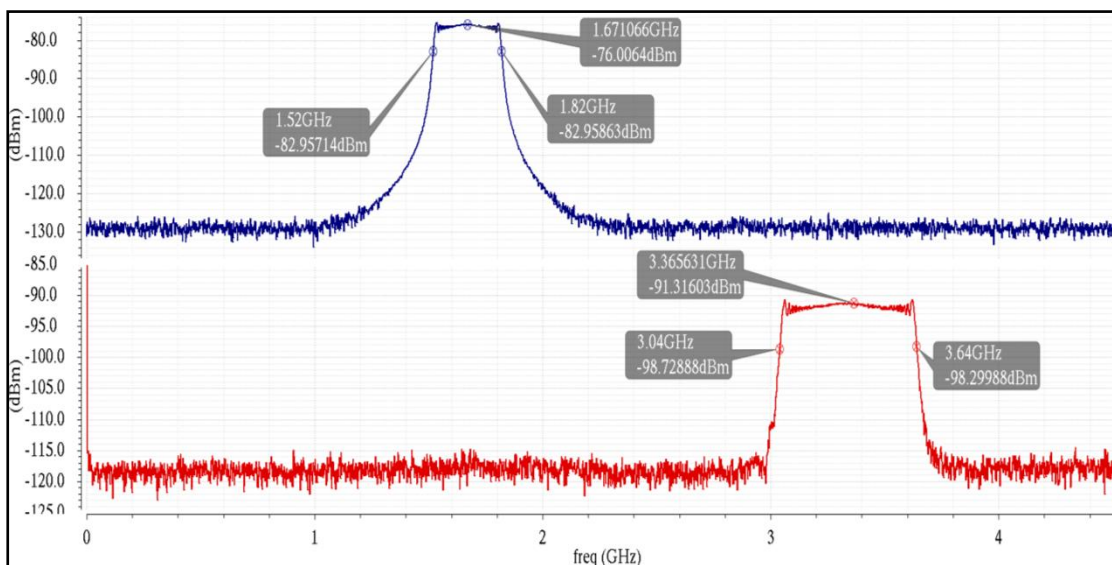


Figure 47: Input (Blue) and Output (Red) Spectrums of Frequency Doubler

6.4 Amplifiers Circuits

6.4.1 Introduction

The amplifier is the stage that is responsible for amplifying signal level. Amplifiers are usually divided into three main categories: Power amplifiers, IF amplifiers, and Low noise amplifiers. The simplest form of an amplifying stage is the common source amplifier. Common source amplifiers are well known in the amplifiers literature, for which there are many references such as [22], [23], [24],

which include proof and detailed analysis for this topology, even though it is still worth mentioning to have a brief overview about common source amplifiers for induction purposes. Figure 48 shows a typical common source amplifier with a resistive load. The gain of the amplifier can be obtained by both small signal and large signal analysis, making sure that the transistor in the circuit is biased in saturation region, the gain can be given by equation (46).

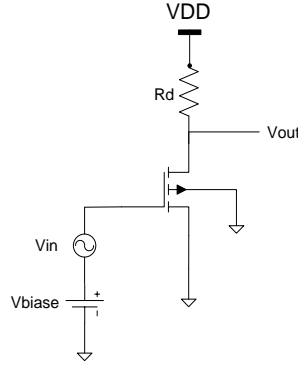


Figure 48: Common source amplifier with resistive load

$$A_v = - g_{m_1} R_{out} \quad (46)$$

where g_{m_1} stands for the amplifier transconductance, as it is given by equation (47). R_{out} stands for the output resistance and it is given by equation (48).

$$g_{m_1} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_d} \quad (47)$$

$$R_{out} = (r_{o_1} \parallel R_d) \quad (48)$$

$$r_{o_1} = \frac{1}{\lambda I_d} \quad (49)$$

From equation (46), it can be noticed that the amplifier gain depends mainly on both the output resistance and the transconductance values; therefore the highest gain can be obtained by having the highest product of the transconductance and the output resistance. However, this isn't as trivial as it looks because to increase the transconductance, it requires either higher current or higher W/L ratio, and the output resistance depends on r_{o_1} value, which consequently depends on the current value.

By increasing the current, we can increase gm but at the same time decrease ro_1 . On the other hand, increasing W/L increases the transistor capacitance and degrades the frequency response of the amplifier.

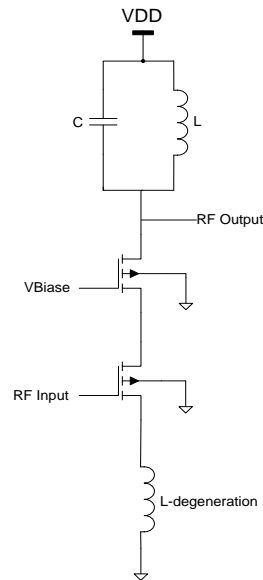


Figure 49: Cascode Amplifier

It is very often to include a common gate stage to enhance the frequency response of the amplifier; a common source amplifier with a common gate amplifier are usually denoted as cascode amplifiers. Figure 49 shows a cascode amplifier circuit. Cascode amplifiers are well known for their high insulation and stability.

An LC tank can be used as a load in narrowband applications, it boosts the gain at the desired frequency of operation and attenuate all other out of band signals. In other words it helps to some extent in the filtration process. Also, a tail degeneration inductor at the source can be used to enhance the linearity of the amplifier.

A second buffer stage can be provided in the design of an amplifier. A simple source follower circuit will function as a buffer and will ease the process of impedance matching at the output port.

There are different ways to measure the stability of a circuit; one way is to use the K stability factor and the auxiliary B_1 factor, the K and B_1 factors can be found from the S parameters of the circuit as given by equations 50 to 52 [25].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (50)$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (51)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (52)$$

The condition for unconditional stability regardless of the source or load impedance of the circuit is guaranteed by the following conditions:

$$K > 1 \quad (53)$$

$$B_1 > 0 \quad (54)$$

6.4.2 First IF Amplifier Circuit

Figure 50 shows the first IF amplifier circuit design. The topology uses a cascode amplifier with an LC tank load centered at 760 MHz. The cascode stage provides higher insulation and better stability. Also, it enhances the frequency response of the amplifier circuit. The LC tank load provides a narrow band operation, which also helps in the filtration process; an inductive degeneration is provided to increase the linearity. The resistance of the inductor helps in the impedance matching by providing the real part of the impedance. A capacitor was inserted at the input of the amplifier to reduce the imaginary part of the input impedance to ease the impedance matching process. The amplifier is followed by a source follower circuit which acts as a buffer stage.

The amplifier provides a high linearity performance. at the expense of high current consumption (an overall 23.9 mA). Also, the noise figure of the stage is relatively high (around 13 dB), however, it doesn't affect the overall system performance as it doesn't appear in the first stages of the system.

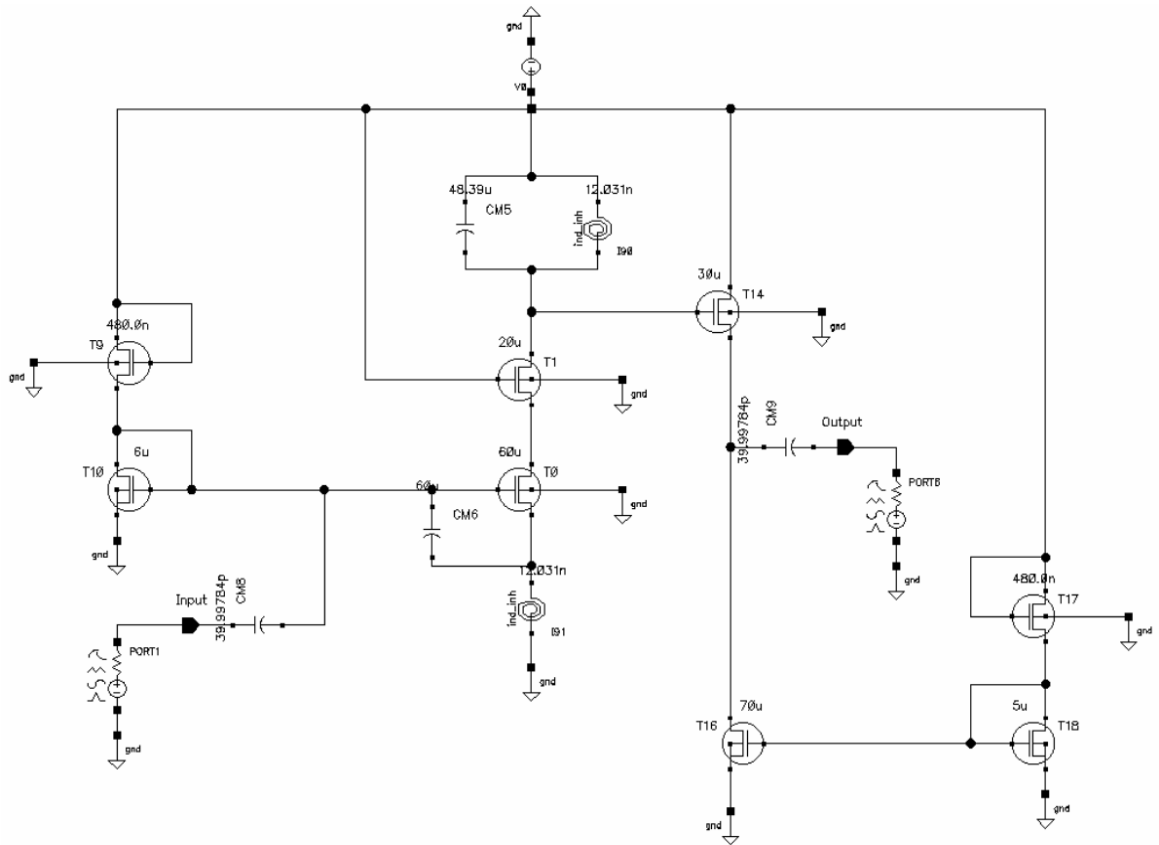


Figure 50: First IF Amplifier Circuit

Figure 51 shows the transient response for both input (red) and output (violet) of the IF amplifier circuit, a gain of around 3.4 V/V is achieved.

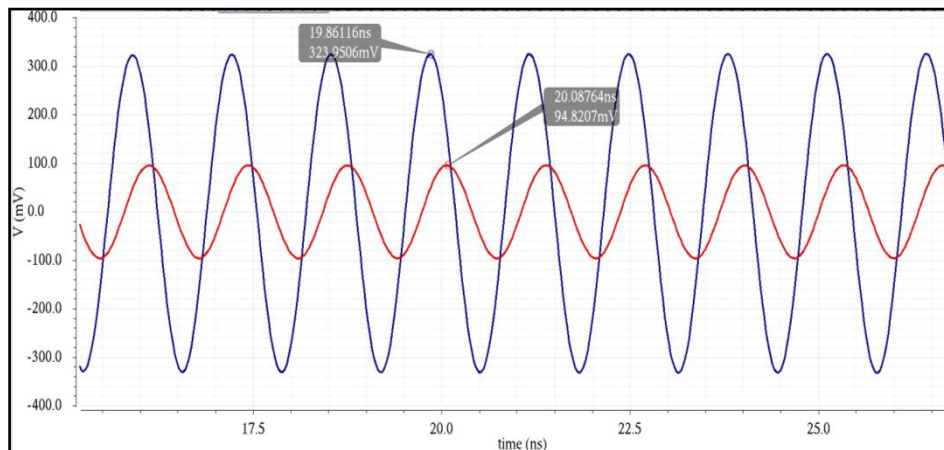


Figure 51: Transient Input (Red) and Output (Blue) of First IF Amplifier Circuit

Figure 52 shows the frequency response of the first IF amplifier circuit. The response provides a gain of 10.886 dB at 760 MHz, and shows that it attenuates the

signals at other frequencies, therefore, it helps in the filtration process of the undesired frequencies.

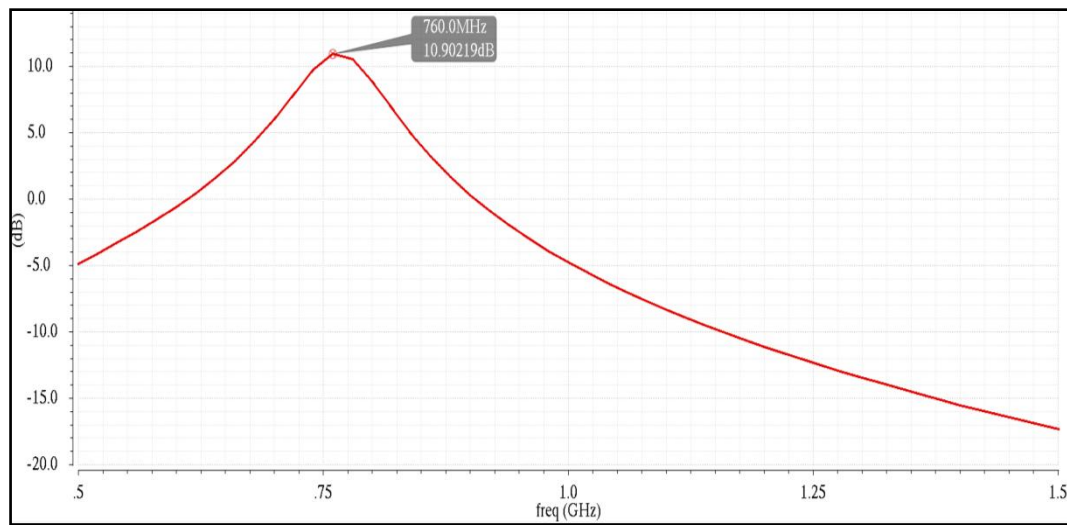


Figure 52: First IF Amplifier Frequency Response

Figure 53 shows a zoomed version of the frequency response in the range between 750 MHz and 770 MHz. It shows that the frequency response is almost flat within the required range of operation.

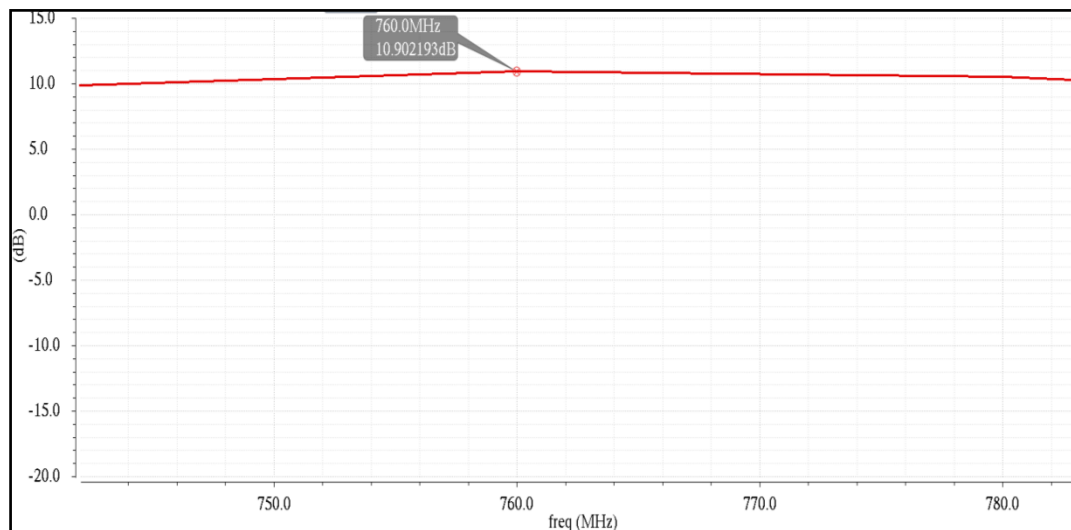


Figure 53: First IF Amplifier Frequency Response from 750 MHz to 770 MHz

Figure 54 shows the linearity test; it shows a 1-dB compression point of -2.97 dBm, the high linearity is accomplished at the expense of drawing higher current.

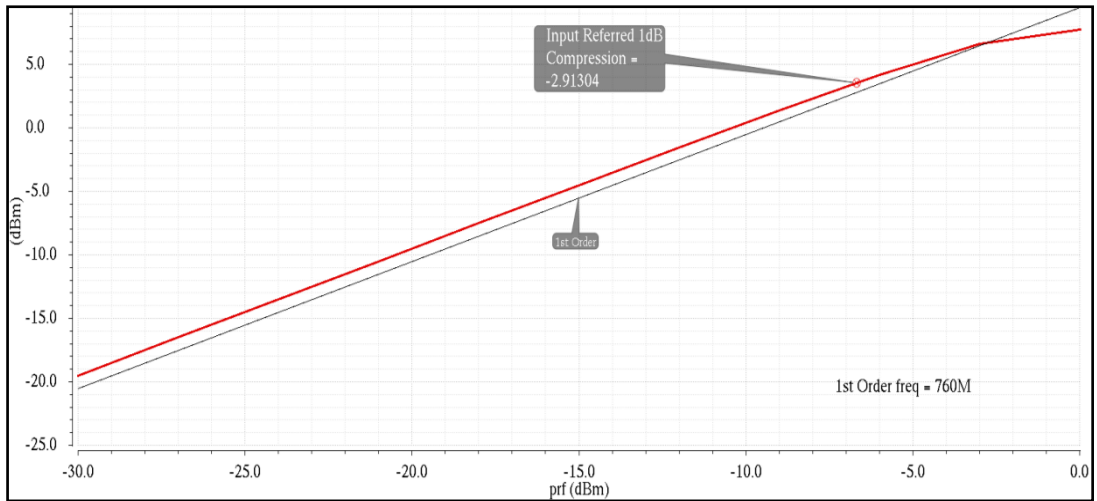


Figure 54: First IF Amplifier 1-dB Compression Point

Figure 55 shows the noise figure, input and output S-parameters. The noise figure value is around 13.4 dB, the S11 is around -25 dB and S22 is around -20 dB which stands for a good impedance matching.

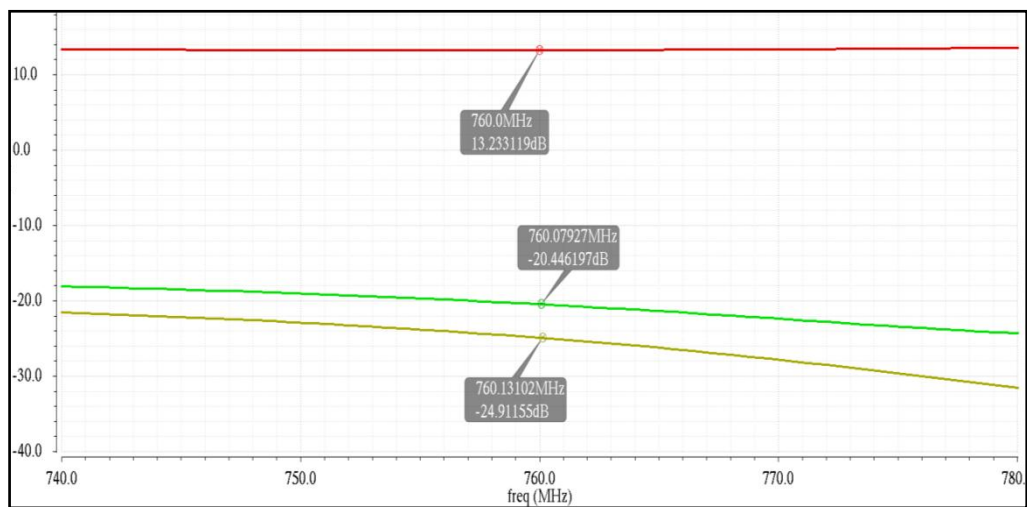


Figure 55: First IF Amplifier S11 (Yellow), S22 (Green) and NF (Red) in dB

Figure 56 and 57 show the K and B_1 factors for testing the stability of the amplifier circuit, the K factor is above 1 and B_1 factor is positive for all frequencies which guarantees an unconditional stability.

Figure 58 shows the input third order intercept point of the amplifier circuit, an 8.5 dBm IIP3 value is achieved.

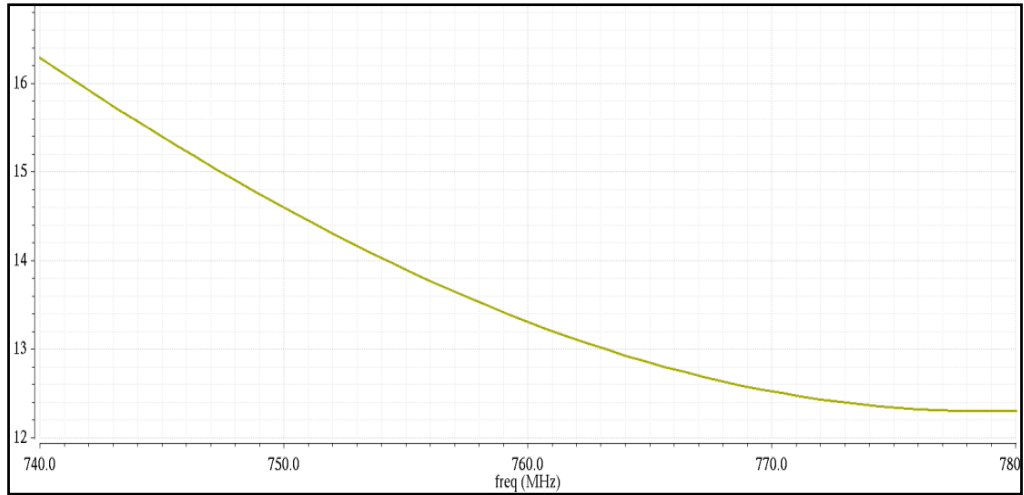


Figure 56: First IF Amplifier K Factor

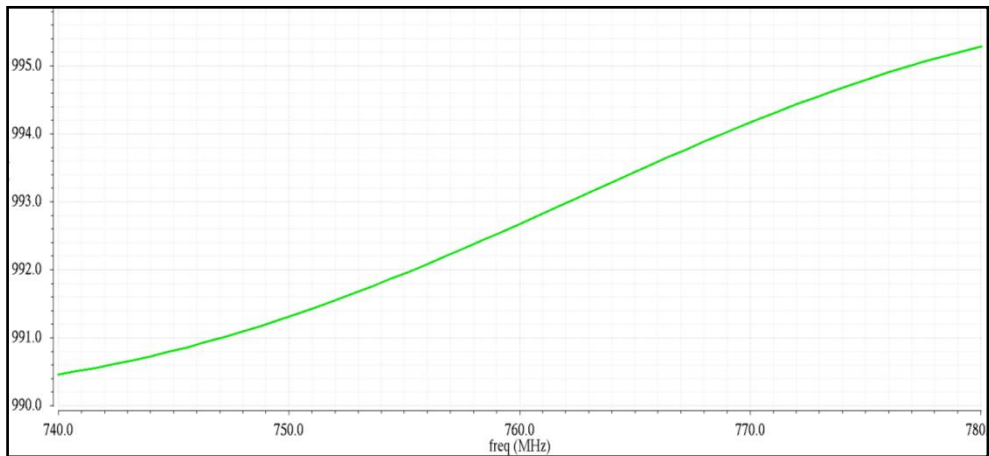


Figure 57: First IF Amplifier B_1 Factor

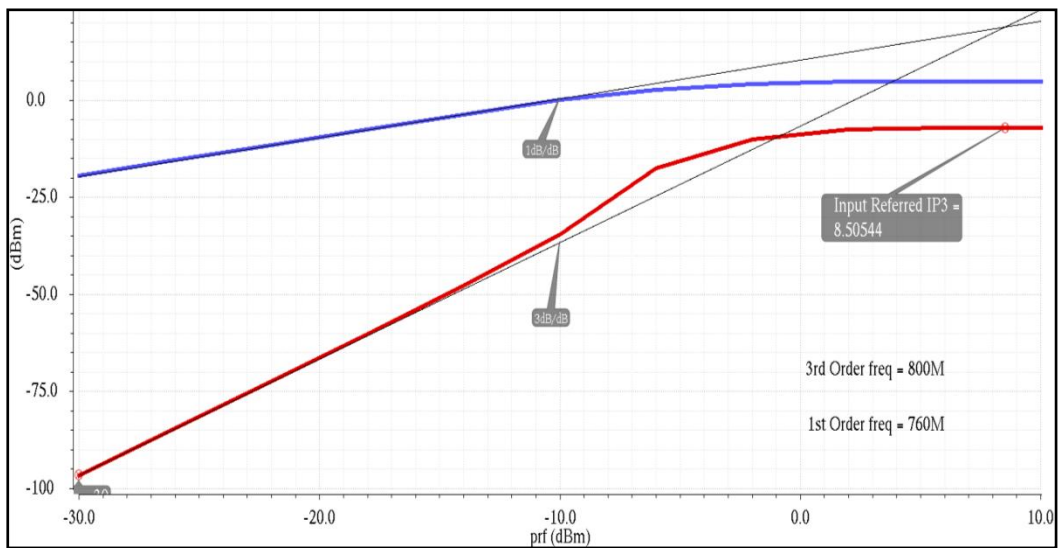


Figure 58: First IF Amplifier Third Order Intercept Point

Table 21: Amplifier (5) Comparison Between Acheived and Required Specs

Parameter	Required Specs	Achieved Specs
Gain (dB)	10 dB	10.9 dB
Noise Figure (dB)	15 dB	13.2 dB
Input 1-dB Compression Point (dBm)	-10 dBm	-2.9 dBm
Input Third Order Intercept Point (dBm)	0 dBm	8.5 dBm
Frequency Range (MHz)	(750 - 770) MHz	

6.4.3 Second IF Amplifier Circuit

Figure 59 shows the circuit design for amplifier 6 which is centered at 70 MHz. The circuit topology is a common source with an active load, a resistive degeneration technique was used to increase the linearity. The degeneration resistor also helped in the input matching process by providing the real part of the input impedance. A capacitor was used across the input to reduce the input imaginary impedance, where a complete matching was achieved with an off chip inductor which eliminates the imaginary part. The common source amplifier stage was followed by a source follower buffer circuit. The output matching was achieved also with an off chip inductor and a small resistance.

Figure 60 shows the transient input (red) and output (blue) of the amplifier, it shows a gain of 3.65 V/V.

Figure 61 shows the frequency response of the second IF amplifier circuit, a gain of 11.2 dB is available at 70 MHz. The frequency response also tend to attenuate the incoming signals existing outside the band of operation, which helps in the filtration process.

Figure 62 shows the frequency response of the amplifier in the range of operation from 62 MHz to 78 MHz. which is almost a flat gain of 11 dB.

Figure 63 shows the noise figure and S-parameters of the second IF amplifier, the noise figure is around 16.8 dB, S11 is -24.7 dB and S22 is -16.5 dB which stands for a good match. Figure 64 and 65 show B_1 and K factors for stability testing. The K

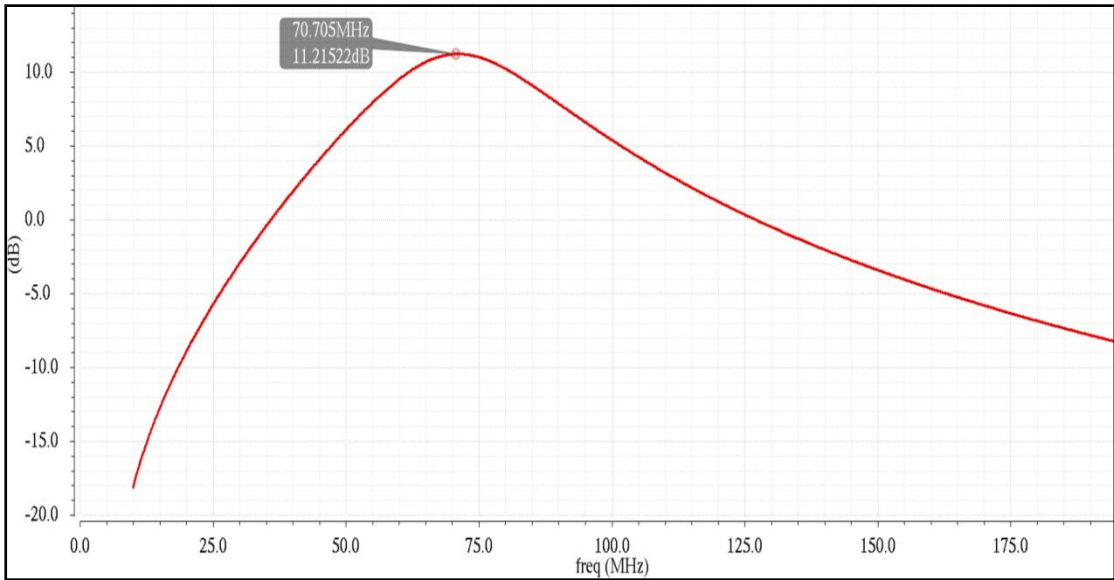


Figure 61: Second IF Amplifier Frequency Response

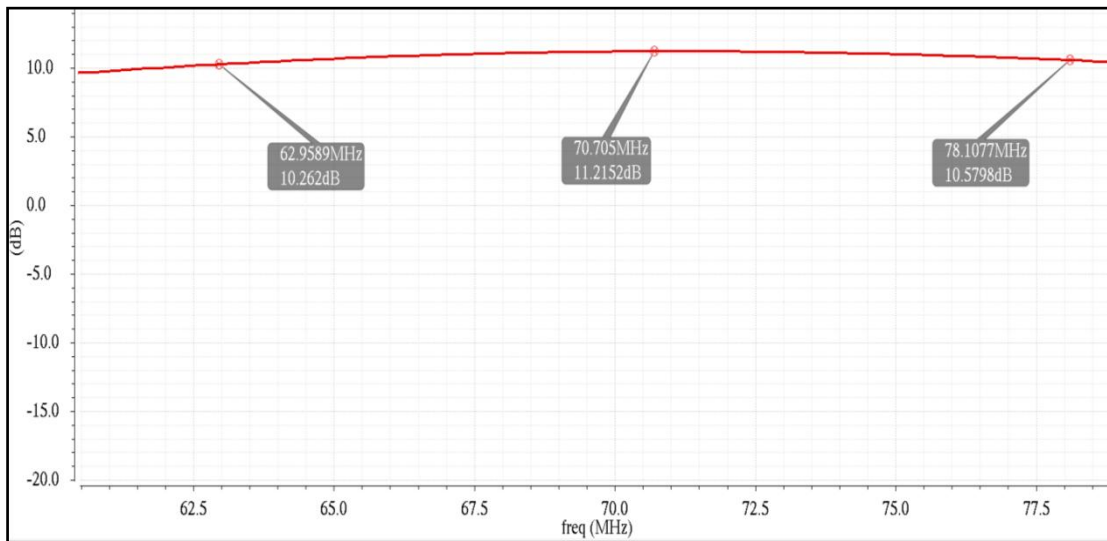


Figure 62: Second IF Amplifier Frequency Response from 62 MHz to 78 MHz

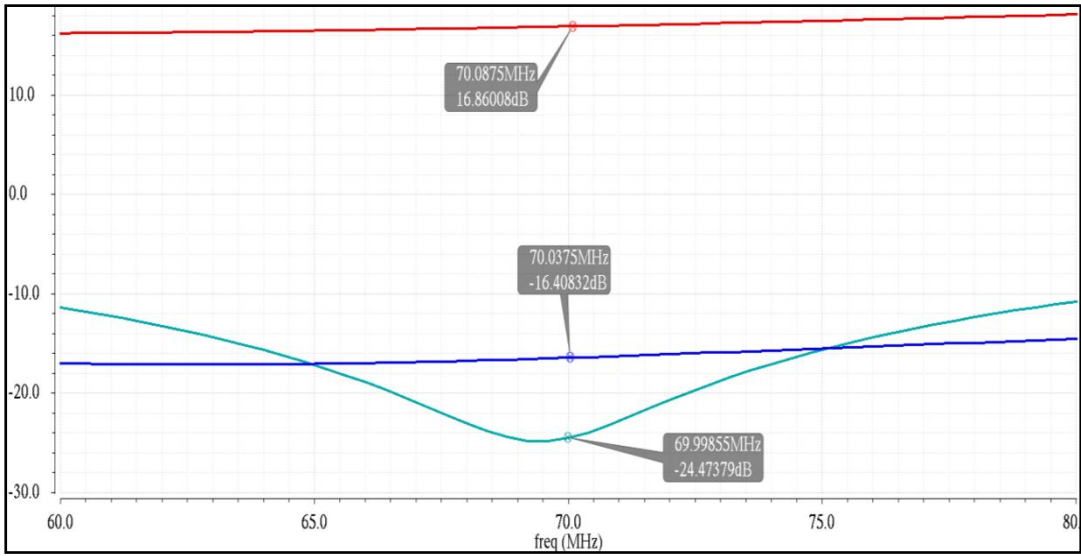


Figure 63: S11 (Cyan), S22 (Blue) and NF (Red) in dB of the Second IF Amplifier Stage

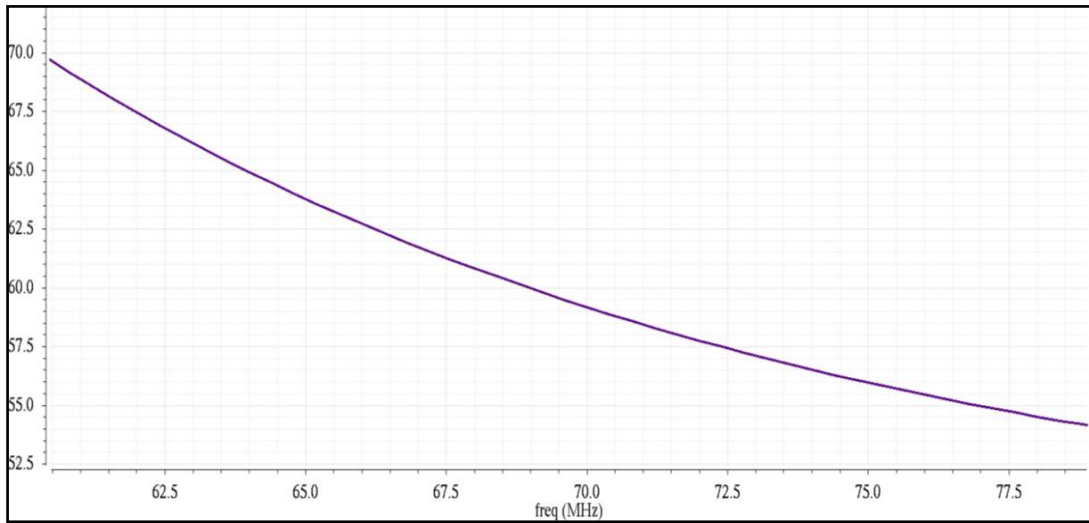


Figure 64: Second IF Amplifier K Factor

Figure 66 shows the linearity test for the 1-dB compression point, a 1-dB compression point of -11.72 dBm is achieved.

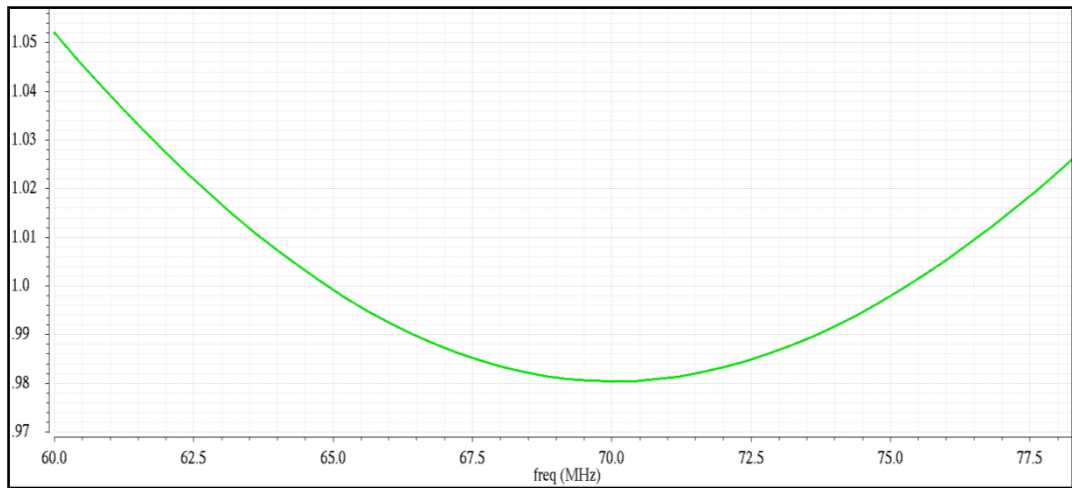


Figure 65: Second IF Amplifier B_1 Factor

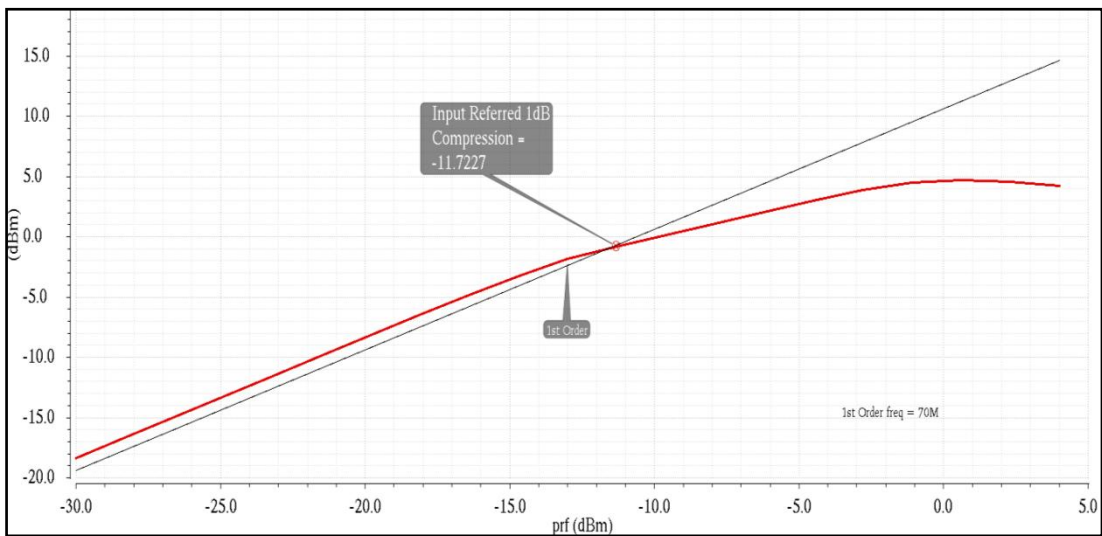


Figure 66: Second IF Amplifier 1-dB Compression Point

Figure 67 shows the third order intercept point of the amplifier, a 1.59 dBm third order intercept point is achieved.

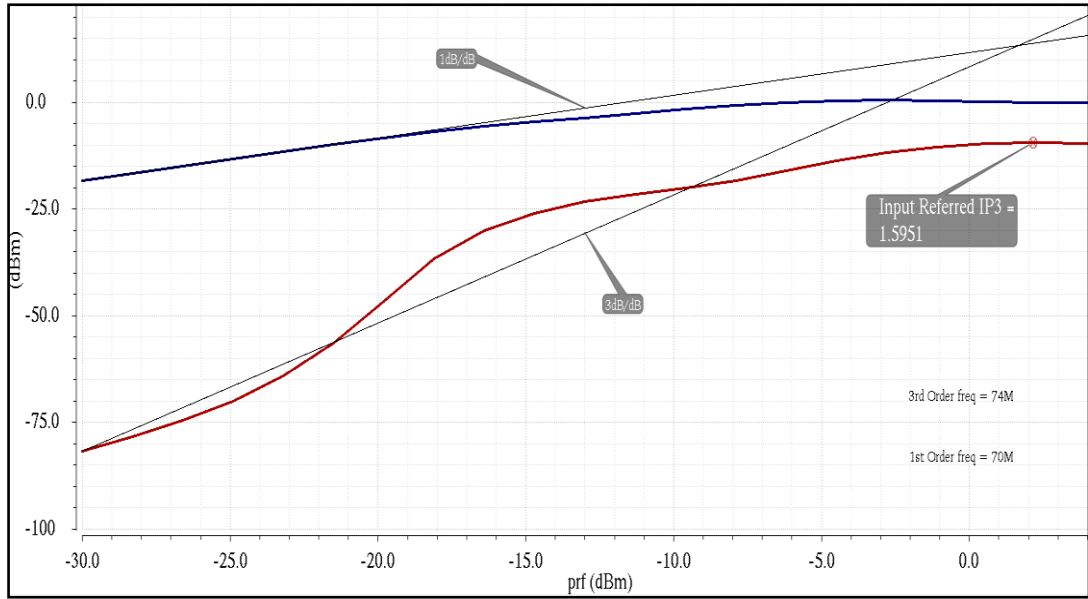


Figure 67: Second IF Amplifier Third Order Intercept Point

Table 22: Amplifier (6) Comparison Between Acheived and Required Specs

Parameter	Required Specs	Achieved Specs
Gain (dB)	11 dB	11.215 dB
Noise Figure (dB)	17 dB	16.86 dB
Input 1-dB Compression Point (dBm)	-10 dBm	-11.72 dBm
Input Third Order Intercept Point (dBm)	0 dBm	1.59 dBm
Frequency Range (MHz)	(62 - 78) MHz	

6.5 Voltage Controlled Oscillator Circuit

An oscillator is a circuit that provides a steady periodic signal at its output. Oscillators are commonly used in modulation and demodulation operations. There are different topologies of oscillators. Negative Gm oscillator is one of the most common topologies used in radio frequency integrated circuits.

To understand how an oscillator works, consider the LC tank circuit shown in Figure 68. This circuit isn't excited by any source; however, white electromagnetic noise exists in the circuit environment. White noise waves can induce a voltage at all frequencies in the circuit according to faraday's law. However, due to the frequency

response of the circuit only one frequency called the resonance frequency can pass through the LC tank and all other frequencies are attenuated. LC tank resonance frequency is given by equation (55). In practice, if a practical measurement were conducted for the circuit, no such voltage or current is observed. This is due to the fact that the inductor and capacitor used are non-ideal components and they possess some resistance that causes the signal to die out. One way to maintain the oscillations from dying is to provide a negative resistance that eliminates the effect of the tank resistance R_T [17].

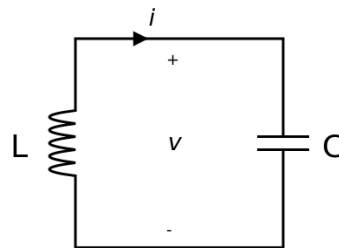


Figure 68: LC tank circuit

$$\omega_{osc} = \frac{1}{\sqrt{LC}} \quad (55)$$

Figure 69 shows a negative gm cross coupled oscillator circuit. The cross coupled transistors at the bottom will provide the negative resistance that will sustain the oscillations and prevent them from dying out due to the tank resistance. It can be shown by performing small signal analysis for the cross coupled pair that they exhibit an equivalent impedance of $(-2/gm)$, therefore, to sustain the oscillations, the cross coupled pair negative resistance should be larger than the tank resistance, equation (56) summarizes the condition of oscillation [17].

$$gm \geq \frac{2}{R_T} \quad (56)$$

To describe the quality of oscillations, the oscillations are required to be available at a single frequency. However, due to the non ideality of the LC tank some other frequencies appear in the oscillator output, the level of these frequencies should

be as minimal as possible, and usually these extra frequencies are denoted as phase noise.

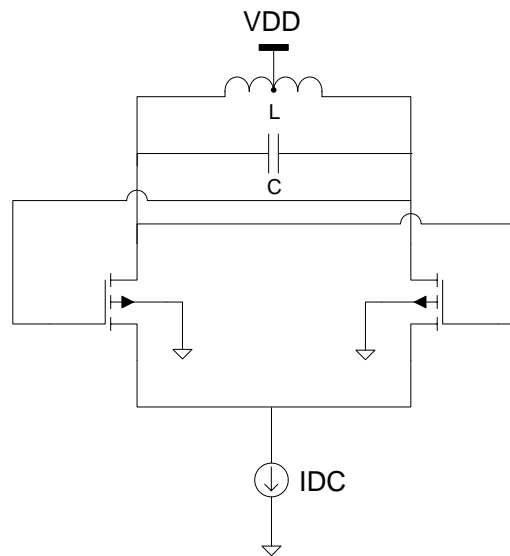


Figure 69: NMOS cross coupled oscillator

To vary the frequency of oscillations, a varactor can be used to change the equivalent capacitance of the tank and hence the frequency of oscillations. There is a variety of varactors. The most common is the NMOS varactor where both drain and source are connected together, and the variable capacitance is seen between the gate and the drain/source. The total NMOS capacitance can be controlled by the gate voltage [17].

Figure 70 shows the VCO circuit design (Oscillator 3 operating at 830 MHz). The circuit uses a negative cross coupled topology. NMOS varactors were used to tune the frequency of oscillations. The VCO was followed by a source follower buffer circuit to accommodate for any loading effects and to ensure stable oscillations frequency. The differential topology provides high immunity against second order harmonic distortion. The VCO circuit is made of three main parts: the LC tank, the cross coupled transistors, and the current mirror biasing circuit. A pulse source was used in the LC tank to initiate the oscillations, the pulse duration lasts for 1 picoseconds and it has an amplitude of 50 mV.

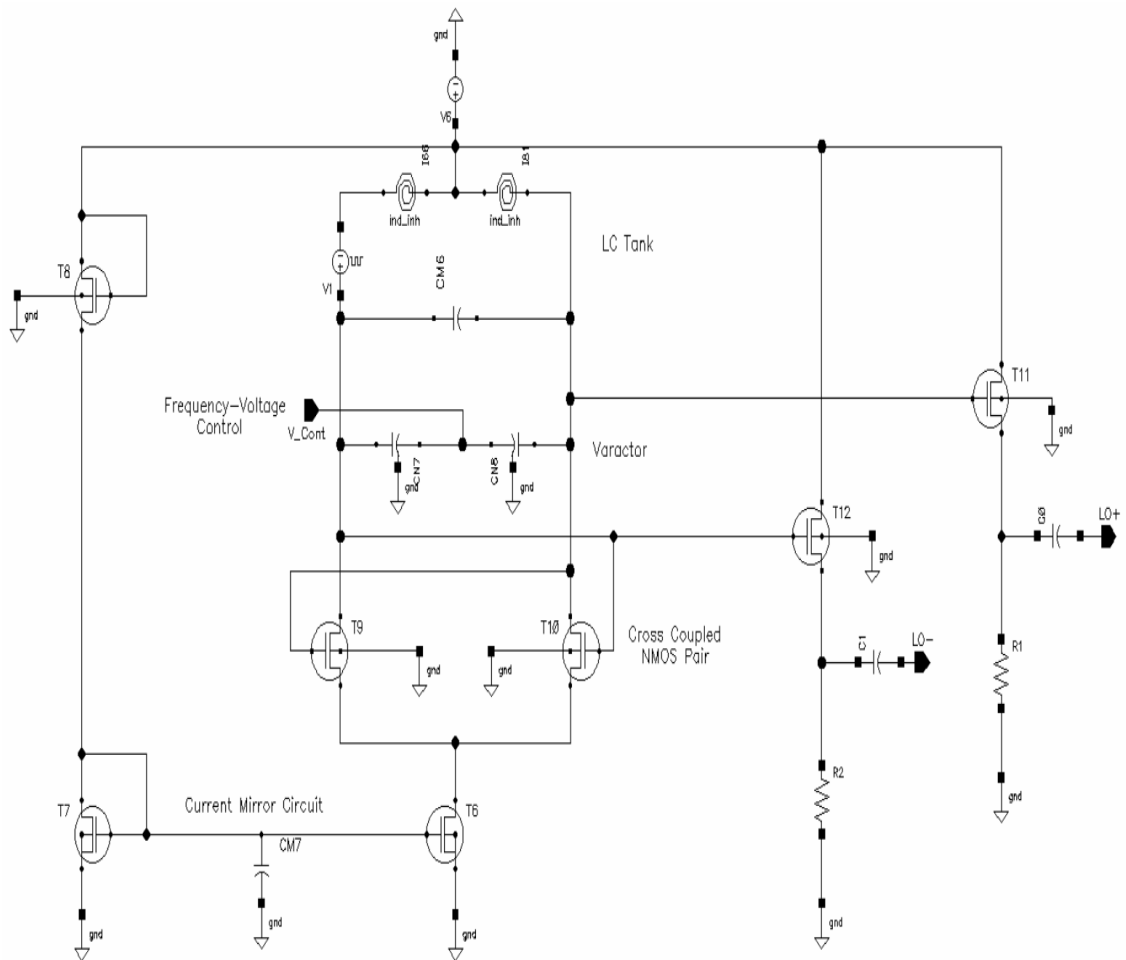


Figure 70: Voltage Controlled Oscillator Circuit

Figure 71 shows the transient output of the VCO circuit. It can be noticed that a stabilization time of 50 nano-sec for the oscillations is achieved. The amplitude of oscillations is around 750 mV peak to peak.

Figure 72 shows the instantaneous frequency of oscillations versus time, the frequency stabilizes to 830 MHz.

Figure 73 shows the oscillations at the positive and negative terminals and also the differential oscillations for both terminals.

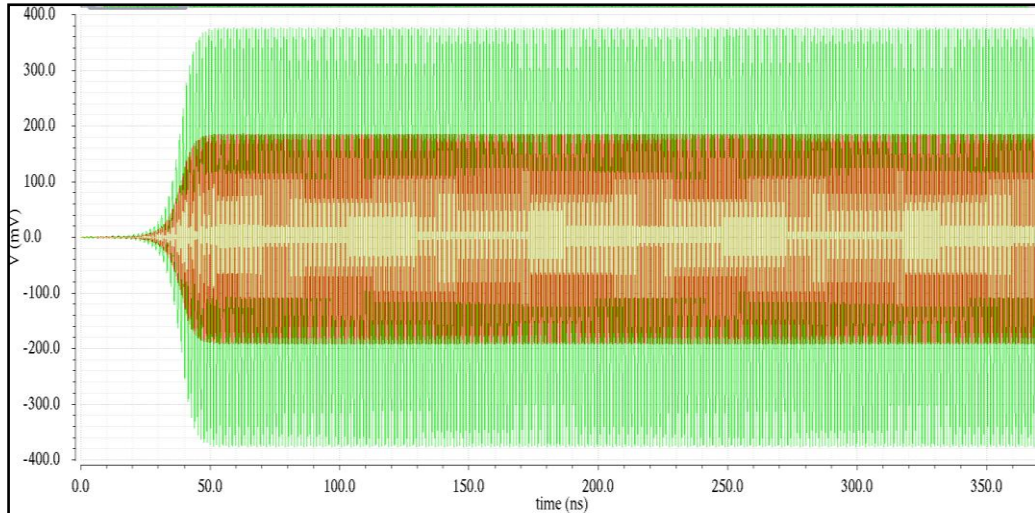


Figure 71: VCO Time Domain Differential (Green) and Single Ended (Brown) Oscillations

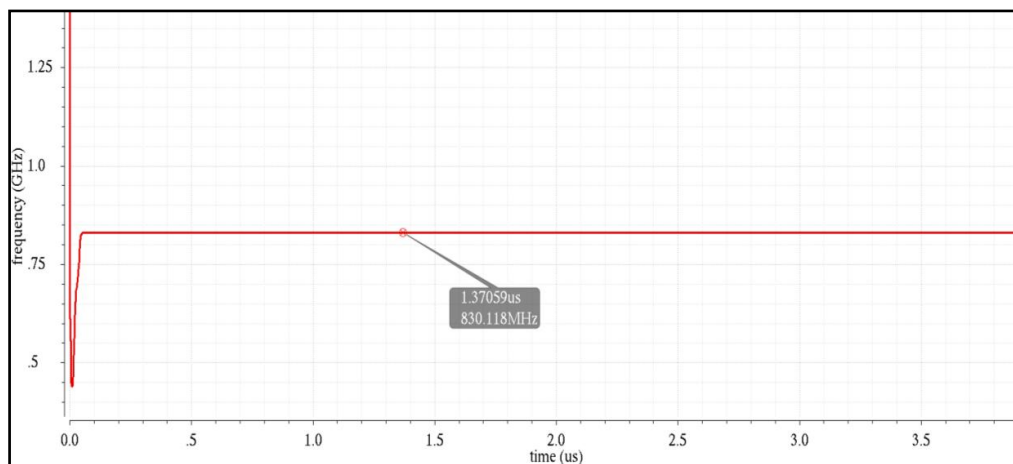


Figure 72: VCO Instantaneous Frequency Vs Time

Figure 74 shows the frequency voltage control of the VCO, the VCO linear frequency range is from 814 MHz to 840 MHz corresponding to a voltage control of 4.85 V to 5.16 V. It can be noticed that the frequency-voltage control curve resembles the same behavior of the NMOS varactor as expected.

Figure 75 shows the VCO gain in the linear region of the VCO. An average of 80 MHz/V VCO gain is achieved.

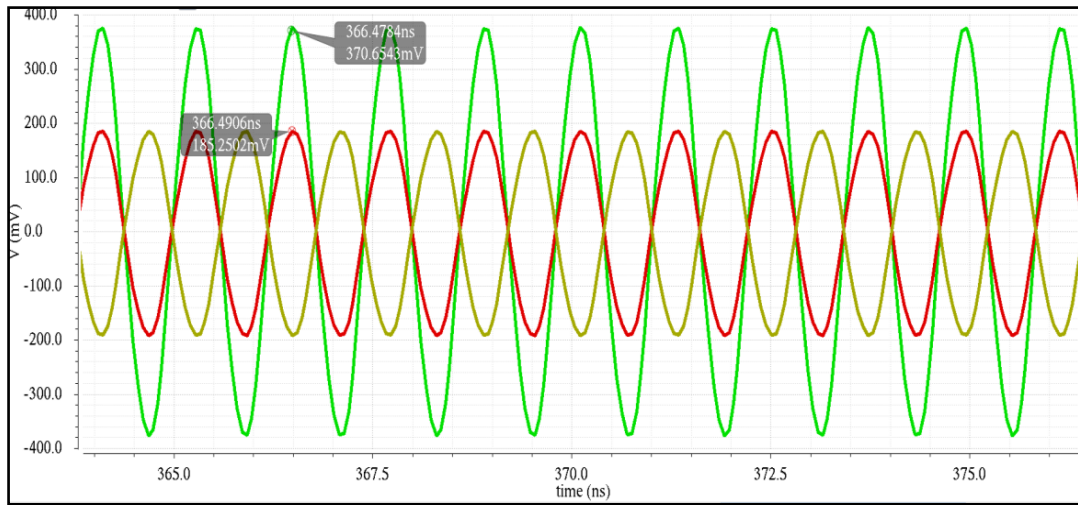


Figure 73: Positive (Red), Negative (Yellow) and Differential (Green) VCO Terminals Output

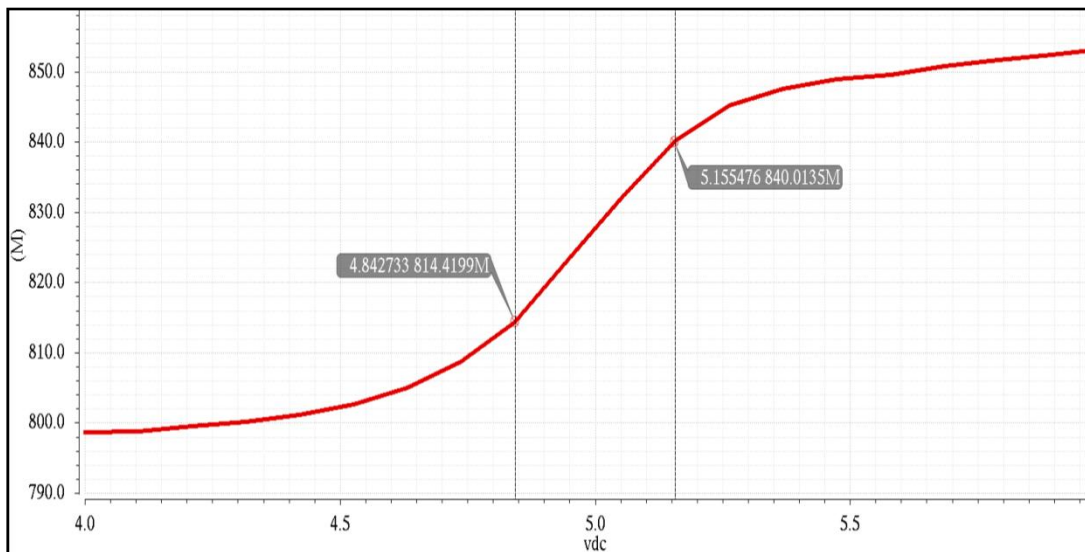


Figure 74: Voltage Control Characteristic of the VCO

Figure 76 shows the phase noise of the VCO, a -23 dBc/Hz is achieved at 1 KHz and a -125 dBc/Hz is achieved at 18MHz.

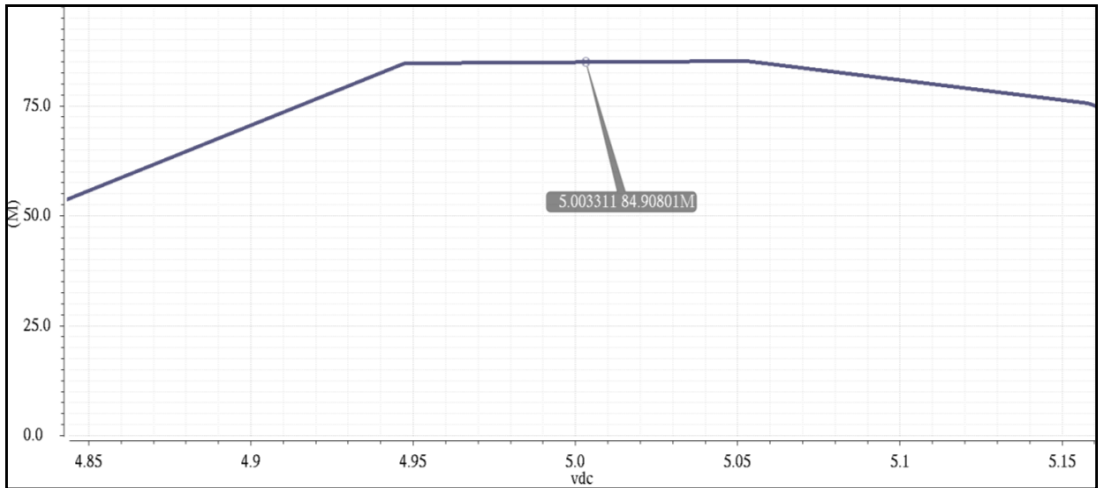


Figure 75: VCO Gain MHz/V

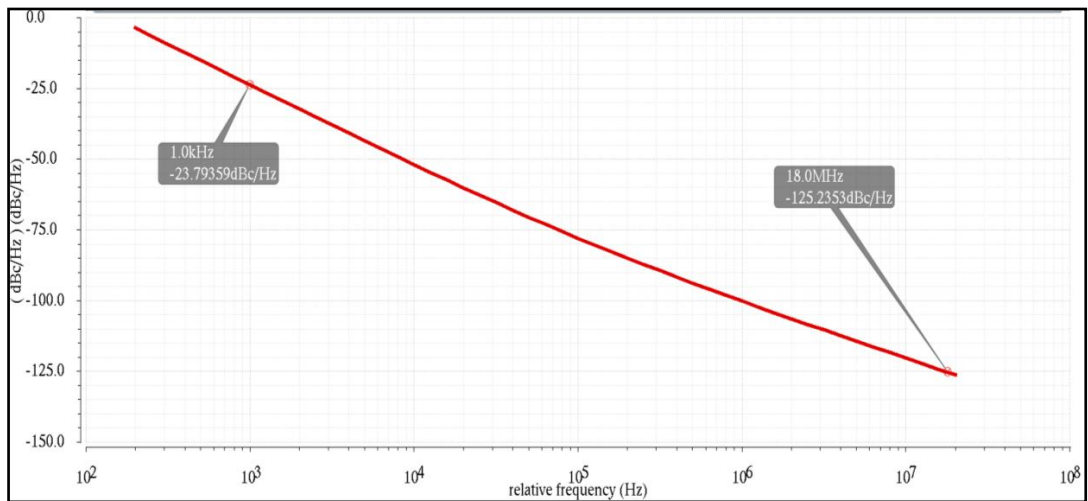


Figure 76: VCO Phase Noise (Center Frequency of 830 MHz)

The circuit FOM was obtained according to equation (57), The phase noise value at 1 MHz is -98 dBc/Hz. The obtained FOM is 165 dB [26].

$$FOM = 10 \log_{10} \left[PN \left(\frac{f_c}{\Delta f} \right)^2 \frac{1}{L(\Delta f) \cdot P} \right] \quad (57)$$

Chapter 7: Receiver System Simulation

After designing, simulating and testing each block of the receiver system at the circuit level individually, all the designed blocks were included in the receiver system and simulated for the final response.

Figure 79 shows the Receiver system including the designed stages at the circuit level. TX and LO Channel chirp signals were used to test the receiver system.

Figure 77 shows the output spectrum of the receiver. It shows a single tone centered at 70 MHz with a dynamic range of 58 dB which complies with the system level simulation.

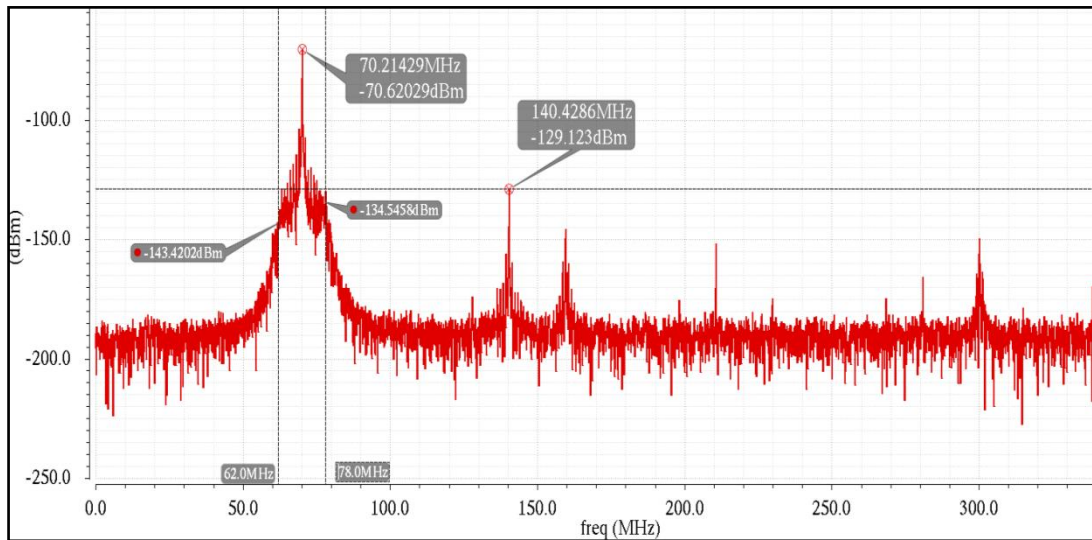


Figure 77: Receiver System Output Spectrum (Slow-Slow Process)

Figure 78 shows the time domain version of the receiver output. As expected, the output shows a single tone with an instantaneous frequency of 70 MHz.

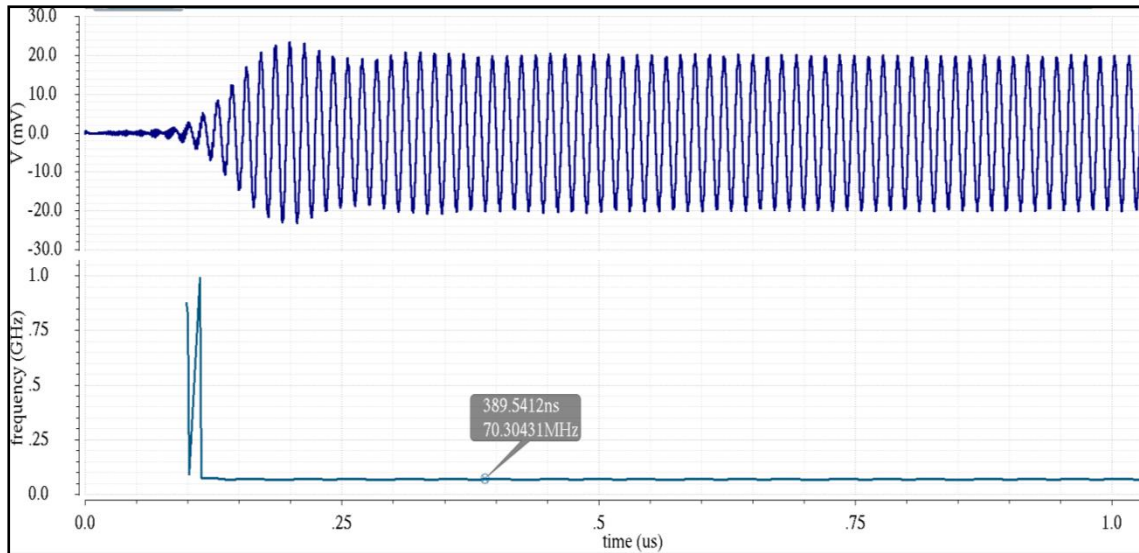


Figure 78: Receiver Time Domain Output and Instantaneous Frequency

Table 23 shows the current consumption of the active stages in the receiver. The total power consumption of the receiver system is 0.323 W.

Table 23: Current Consumption of Active Stages

Stage	Current Consumption
First IF Amplifier	23.9 mA
Second IF Amplifier	13.29 mA
Voltage Controlled Oscillator	27.6 mA

The receiver system was tested over the four corners: slow-slow, fast-slow, slow-fast and fast-fast. The results showed that slow-slow and slow-fast processes gave good dynamic range of 58 dB, however in the fast-slow and fast-fast process the VCO frequency deviated from the intended design frequency. Figure 80 shows the slow-fast process simulation for the receiver output.

Figure 81 shows the output of the second mixer in the receiver chain, as it shows the signal was translated from 760 MHz to 116 MHz rather than 70 MHz. This is due to the shift in the frequency of the VCO from 830 MHz to 876 MHz.

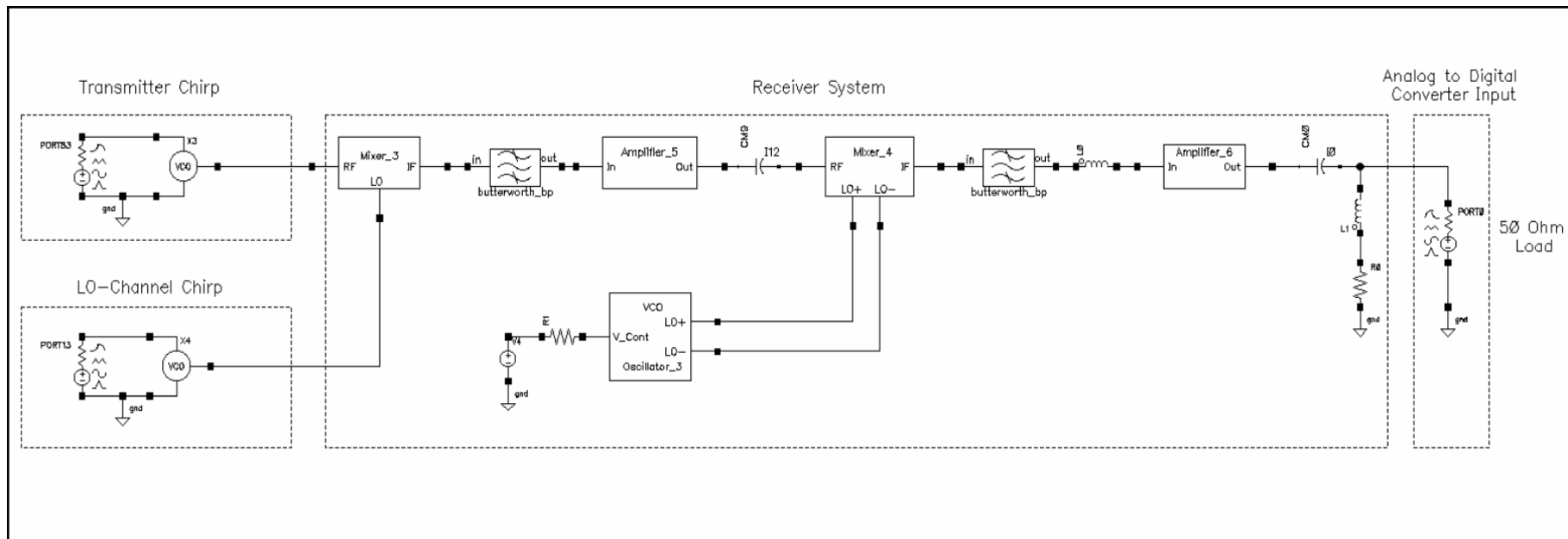


Figure 79: Receiver System Simulation using Designed Blocks

Figure 82 shows the final output of the receiver which filters out the received tone due to its existence outside the band of the last filter in the receiver chain.

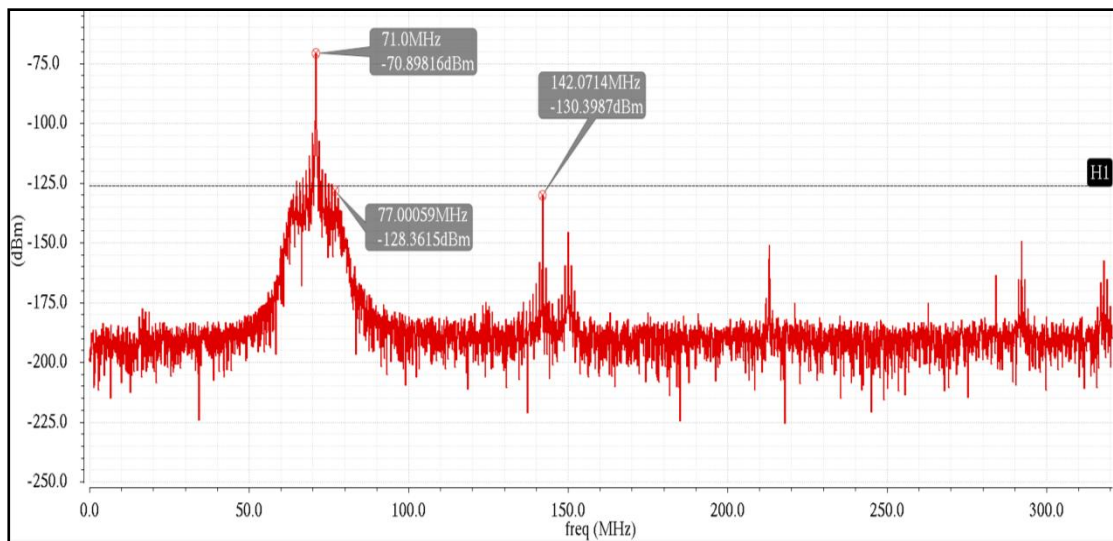


Figure 80: Slow-Fast Process Receiver Output

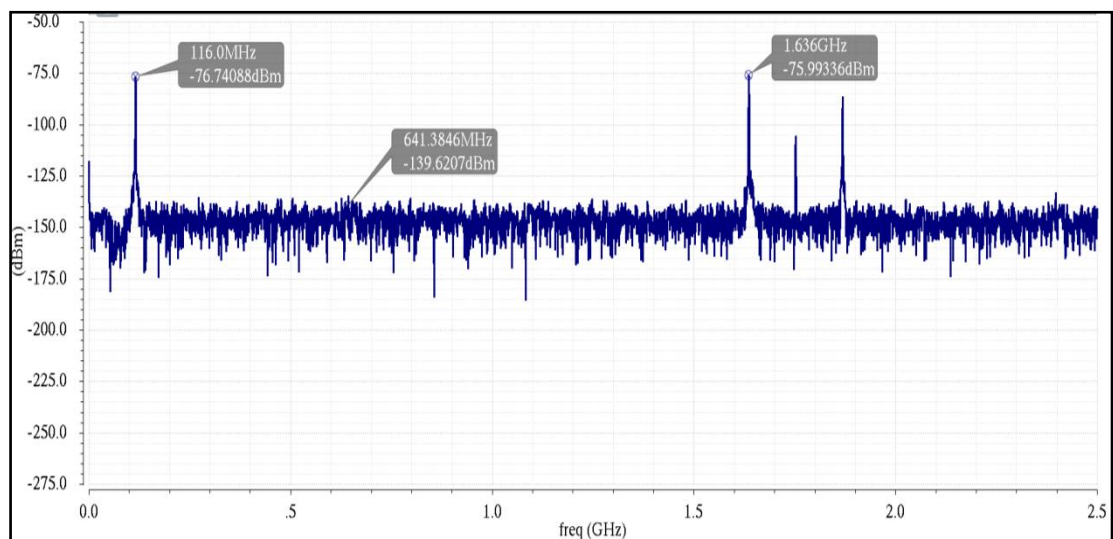


Figure 81: Second Mixer in the Receiver Output (Fast-Slow Process)

This concludes that a phase locked loop system is required for the receiver VCO circuit. Providing a PLL controls the frequency of oscillations and reduces level of drifting. No VCO pulling effect was analyzed in this work. This is a small risk where several VCOs operate on the same chip.

Figure 83 shows the output of the second mixer in the receiver chain in the case of Fast-Fast process. Also, Figure 84 shows the final receiver output for Fast-Fast process.

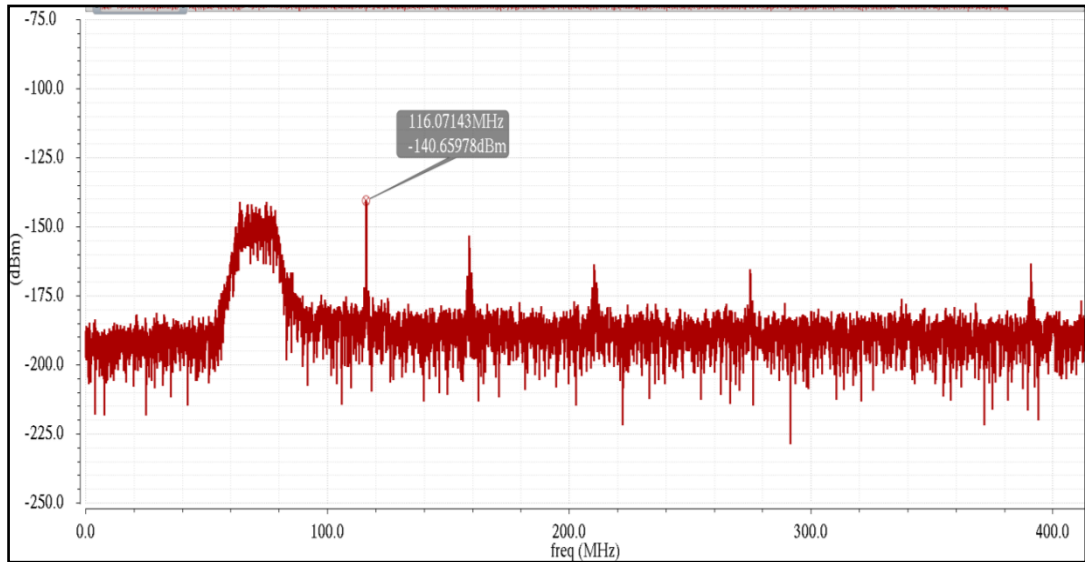


Figure 82: Receiver Output Spectrum (Fast-Slow Process)

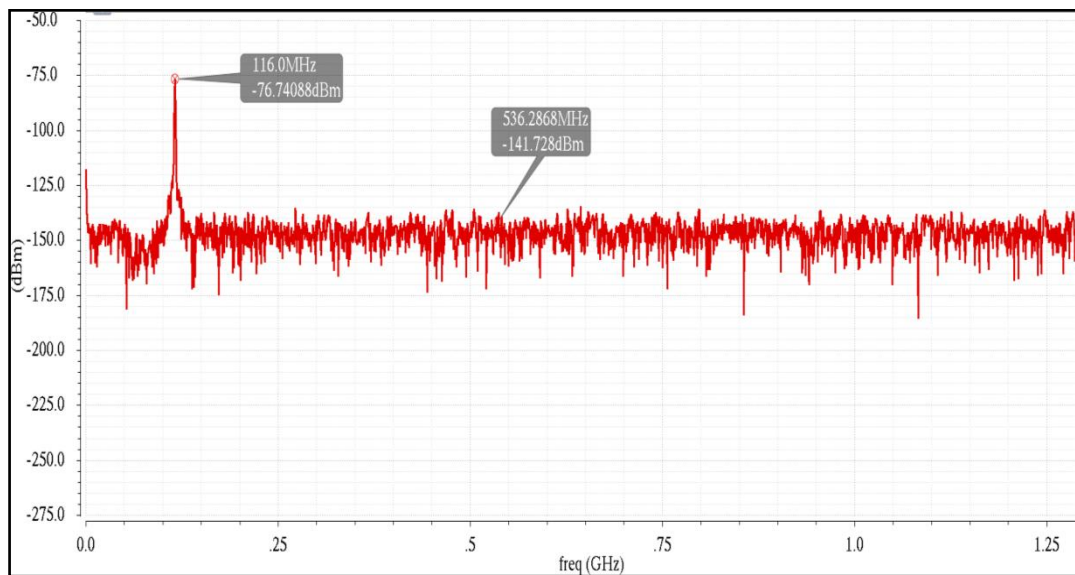


Figure 83: Second Mixer Output (Fast-Fast Process)

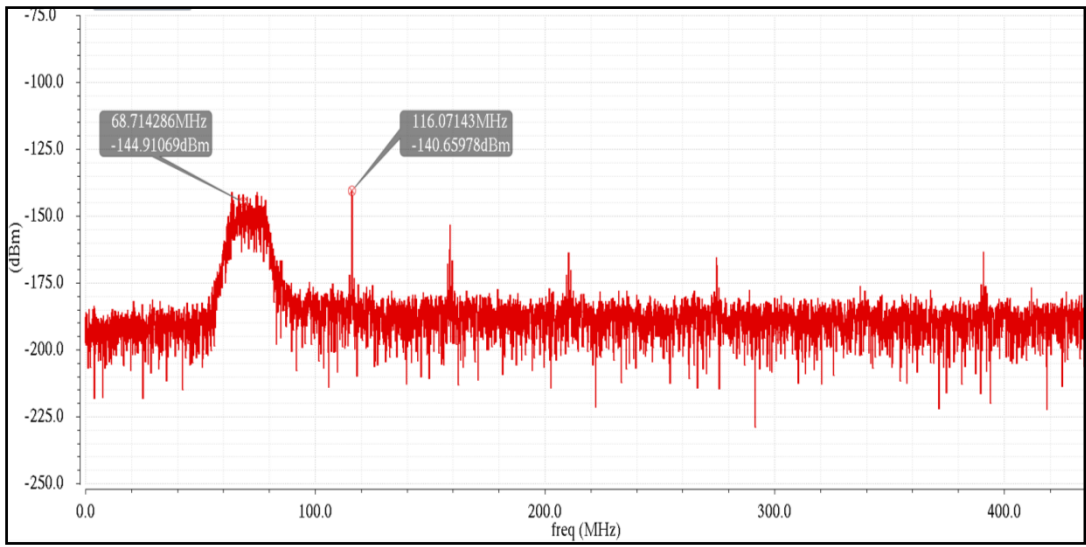


Figure 84: Receiver Output (Fast-Fast Process)

Chapter 8: Conclusion and Future Work

On chip system level design and simulation for a high performance radar was carried out. The system level design provided feasible block specifications for realizing the radar chipset system. The radar system uses stretch processing technique that ensures high resolution (up to 0.25 m) and low sampling rate requirement for analog to digital converters. The radar system has a high dynamic range that ensures high performance operation in the presence of clutter. Using multiple receiver channels enable digital antenna beamforming to mitigate any strong interferer. The radar system operates in the S-Band which provides high immunity against clutter in long range surveillance applications.

Integrating the radar at the chip level provides a small size, low cost, low power consumption and portable solution. The performance of the radar highly depends on the filtration quality (i.e. sharpness and flatness). Integrating sharp and flat filters on chip requires large area, therefore, flat Butterworth filters were assumed to be off chip.

The level of generated spurs after each stage depends on the linearity of each stage. Therefore, to reduce spurs level, high linearity double balanced passive mixers and doublers were considered. Amplification stages were used to accommodate for the signal loss.

The total receiver system of the radar chipset was designed and simulated at the circuit level using Cadence Virtuoso 6.0 on IBM 180 nm CMOS technology; a high dynamic range of 58 dB was achieved and a total power consumption of 0.32 W. Future work can include the circuit design of the transmitter and LO Channel, and realize the chipset prototype. Also, a PLL system can be designed for the VCO circuit to ensure the stability of required oscillations frequency against process variations.

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Appendix (A) Beamforming Example MATLAB Code

```
% This code demonstrates the beamforming concept, A linear array of
% 5 antennas with 3 incident signals at different angels, it is required to
% detect the incident angels and beamform the array to a certain angle of
% interest

clc; clear; close all

fc=100; % Carrier Frequency
c=3*10^8; % Speed of Light (i.e. Propagation Velocity)
lam=c/fc; % Wave length (m) Lambda
d=lam/2; % Distance Between Antennas
m=40; % dt resolution factor
dt=1/(m*fc); % Sampling Time Step
t=[0:dt:400]; % Time Span
fs=1/dt; % Sampling Frequency
f=linspace(-fs/2,fs/2,length(t)); % frequency vector
cutoff_freq=40; % Low Pass Cutoff Frequency
w_cut=2*cutoff_freq/fs; % Value to be used in Filter Design

x1=cos(2*t); % Signal 1
x2=cos(3*t); % Signal 2
x3=cos(6*t); % Signal 3

% Plotting the 3 original signals
plot(t,x1);
hold
plot(t,x2,'m');
plot(t,x3,'r');

% angel of incidence of each signal
th1=-40*(pi/180); % Theta 1 for signal 1 in radians
th2=0*(pi/180); % Theta 2 for signal 2 in radians
th3=40*(pi/180); % Theta 3 for signal 3 in radians

% Steering Vector for each signal (i.e. providing time shift for each
% antenna)
v1=[1 exp(-i*2*pi*fc*d*sin(th1)/c) exp(-i*2*pi*fc*2*d*sin(th1)/c) exp(-
i*2*pi*fc*3*d*sin(th1)/c) exp(-i*2*pi*fc*4*d*sin(th1)/c)];
v2=[1 exp(-i*2*pi*fc*d*sin(th2)/c) exp(-i*2*pi*fc*2*d*sin(th2)/c) exp(-
i*2*pi*fc*3*d*sin(th2)/c) exp(-i*2*pi*fc*4*d*sin(th2)/c)];
v3=[1 exp(-i*2*pi*fc*d*sin(th3)/c) exp(-i*2*pi*fc*2*d*sin(th3)/c) exp(-
i*2*pi*fc*3*d*sin(th3)/c) exp(-i*2*pi*fc*4*d*sin(th3)/c)];

% Received Signals for each incident signal after applying steering vector
X1=[x1*v1(1); x1*v1(2); x1*v1(3); x1*v1(4); x1*v1(5)]; % X1=x1*v1
X2=[x2*v2(1); x2*v2(2); x2*v2(3); x2*v2(4); x2*v2(5)]; % X2=x2*v2
X3=[x3*v3(1); x3*v3(2); x3*v3(3); x3*v3(4); x3*v3(5)]; % X3=x3*v3
```

```

% Generating White Gaussian Noise
E=trapz(t,double(X1(1,:).^2));
SNRdB=100;
N=E*10.^(-SNRdB/10);
w=randn(5,length(X1))*sqrt(N*fs/2);

% Receiver Total Output (i.e. for each antenna)
X=X1+X2+X3+w;

% Calculating Spatial correlation matrix Rx
kf=size(X);
kf=kf(2);
Rx=0;
for k=1:kf
Rx=Rx+X(:,k)*X(:,k)';
end
Rx=Rx/kf;

% Eigen Values and equivalent vectors for Rx
eig(Rx)
[V,D]=eig(Rx);

% Determining H matrix (optimizing the detection of a certain angel)
h=inv(Rx)*v2; % Choose signal 1 put (v1) signal 2 (v2) and so on..

% Applying H matrix and plotting
y=h'*X;
plot(t,(y)/max(y),'*')
xlim([0 6])

% Received signal without applying the H matrix (i.e. without beamforming)
plot(t,abs([1 1 1 1 1]*(X)),'g') % Signal with h=1 (i.e. no beamforming)
xlim([0 6])

xlabel('Time(Seconds)'); ylabel('Signal Level');
legend('Original Signal (1)','Original Signal (2)','Original Signal (3)','After
beamforming','Before beamforming');

% obtaining Uw egin vectors (corresponding to small egin values)
Uw=[V(:,1) V(:,2)];
th=[-90*pi/180:0.01:90*pi/180];

% determining incident angels
for m=1:length(th)
vth=[1 exp(-i*2*pi*fc*d*sin(th(m))/c) exp(-i*2*pi*fc*2*d*sin(th(m))/c) exp(-
i*2*pi*fc*3*d*sin(th(m))/c) exp(-i*2*pi*fc*4*d*sin(th(m))/c)];
A(m)=1/norm(Uw'*vth); % incident angle
A2(m)=(h'*vth); % beam pattern
end

```

```
figure
plot(th*180/pi,(abs(A)))
xlabel('Angel(degrees)'); ylabel('Detected Angles');
figure
plot(th*180/pi,abs(A2))
xlabel('Angel(degrees)'); ylabel('Rx Gain');
```

Vita

Yazan Al-Alem earned his B.Sc degree in Electrical Engineering from the *University of Jordan* in 2010, after which he joined *United for Telecom Services company* as a site engineer. He participated in the survey, installation and drive test phases of Zain - Huawei 3G⁺ Mobile Broadband project in Jordan. Later, he joined *the Blue Zone East company* where he worked as a technical support engineer for the Wi-Max IEEE 802.16e internet service. In the period 2011 – 2013, he joined *Dar Al-Handasah Consultants* where he worked as an Electrical Design Engineer. He worked on the design of various systems, including the design of indoor distributed antenna systems, sound systems and lighting systems. The main projects he worked on included: the Custodian of the two holy mosques king Abdullah Bin Abd Al-Aziz project for increasing Tawaf "circling" capacity (KSA-Mecca) and Bahrain international airport terminal expansion project. In 2013 he was granted a graduate teaching assistantship at the *American University of Sharjah* to complete his M.Sc degree in Electrical Engineering.