Miniaturized Low-Cost High-Performance Digital Radar

MINIATURIZED LOW-COST HIGH-PERFORMANCE DIGITAL RADAR

by

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Abstract

Digital radars offer added advantages and functionality such as higher stability and precision compared to conventional radar systems. By utilizing multiple receiver channels, digital array radars (DARs) are able to perform several functions such as tracking a specific target in space, while rejecting jammers from a certain angular location (known as spatial filtering). This is of interest in high clutter environments such as coastlines. This study aims to miniaturize a cutting-edge digital radar testbed implemented using discrete microwave components, developed earlier at the American University of Sharjah. The main objectives of the thesis are to achieve a level of practical portability for the system without compromising the overall performance and to maintain a low cost budget. Furthermore, this study presents several characteristics of digital radars and discusses the limitations and constraints faced during their design and implementation phases. The novel architecture design and implementation process of the miniaturized low-cost and high-performance S-band digital radar is presented. The proposed system is simulated through multiple software platforms including advanced design system (ADS) and advancing the wireless revolution's (AWR) visual system simulator (VSS). This report details the design and full-wave EM simulation of different types of filters specifically designed to be implemented in the radar testbed. It also explains the impedance matching procedure followed in order to minimize power losses. The overall system is first designed for the standard low-cost printed circuit board (PCB) technology, then simulated using the aforementioned software, and finally fabricated. The implemented radar testbed utilizes the stretch processing technique in order to achieve a high dynamic range over a wide signal bandwidth. The experimental measurements of the fabricated radar testbed verify a high in-band dynamic range of 75 dB across an instantaneous bandwidth of 600 MHz, corresponding to 0.25 meters of range resolution. The achieved high dynamic range is unique and has not yet been explored for the miniaturized scale of digital radar testbeds.

Search terms— Digital Radar; Range Resolution; Dynamic Range; Stretch Processing; RF System Frequency Plan; Microwave Planar Filters; RF System Architecture and Circuits.

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List of Abbreviations

AC	-	Alternating Current
ADC	-	Analog-to-Digital Converter
ADS	-	Advanced Design System
AGC	-	Automatic Gain Control
AWG	-	Arbitrary Waveform Generator
AWR	-	Advancing the Wireless Revolution
BPF	-	Band Pass Filter
CC	-	Capacitively-Coupled
CDR	-	Compression Dynamic Range
CL	-	Coupled Line
CMOS	-	Complementary Metal-Oxide Semiconductor
COTS	-	Commercial Off-the-Shelf
DAC	-	Digital-to-Analog Converter
DAQ	-	Data Acquisition
DAR	-	Digital Array Radar
DC	-	Direct Current
DDS	-	Direct Digital Synthesizer
DGS	-	Defected Ground Structure
DSB	-	Double Side Band
EM	-	Electromagnetic
FIR	-	Finite Impulse Response
FMCW	-	Frequency Modulated Continuous Wave
FR4	-	Flame Retardant-4
I/O	-	Input/Output
IC	-	Integrated Circuit
IF	-	Intermediate Frequency
ILDR	-	Ideal Linear Dynamic Range
IMD	-	Intermodulation
IP3	-	Third-Order Intercept Point
IQ	-	In-phase Quadrature

LFM	-	Linear Frequency Modulated
LNA	-	Low Noise Amplifier
LO	-	Local Oscillator
LPF	-	Low Pass Filter
MDS	-	Minimum Detectable Signal
MIC	-	Microwave Integrated Circuit
NF	-	Noise Figure
PCB	-	Printed Circuit Board
Q	-	Quality Factor
Radar	-	Radio Detection and Ranging
RF	-	Radio Frequency
RX	-	Receiver
SAW	-	Surface Acoustic Wave
SFDR	-	Spurious Free Dynamic Range
SIR	-	Stepped-Impedance Resonator
SNR	-	Signal-to-Noise Ratio
SSB	-	Single Side Band
TX	-	Transmitter
VCO	-	Voltage Controlled Oscillator
VNA	-	Vector Network Analyzer
VSS	-	Visual System Simulator

Chapter 1: Introduction to Radar Systems

1.1 Basic Radar Systems

A radar (*radio detection and ranging*) system is defined as an electromagnetic (EM) surveillance system that is used to scan the environment to detect a target. A typical radar system consists of two major subsystems which are the transmitters and receivers. A signal is generated, processed, and emitted by the transmitter to the surroundings; if there is a target in range, the transmitted energy is partially scattered by the object. In the presence of a target, the receiver gets the signal reflected by the target, which is a time-delayed version of the transmitted signal (Figure 1.1). This time delay is proportional to the distance travelled by the signal [1].

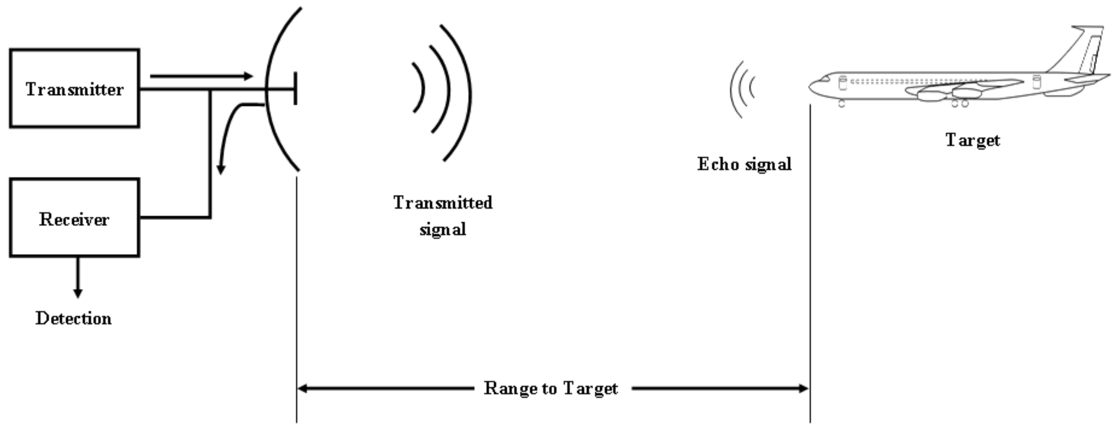


Figure 1.1: Basic principle of radar.

Radars can be classified depending on how the transmitter and the receiver are placed. In monostatic radars, the same antenna is used for transmission and reception of the signal, while in multistatic radars, the transmitter and receiver are separated [2]. In addition, there are several categories of radars based on their applications, such as surveillance radars, airport vehicular monitoring radars, speed measurement radars, ground-based weather radars, airborne weather-avoidance radars, altimeter radars, space application radars, and cross-section test range radars [3].

Typical conventional radar systems utilize a series of short pulses in order to measure the range of the surrounding objects. These signals travel with the speed of light ($c = 3 \times 10^8\ m/s$) in the free space medium. Hence, the range to the target can be obtained by

$$R = \frac{c\,T_R}{2} \tag{1.1}$$

where T_R is the time that it takes to receive the reflected version of the transmitted signal (echo) at the radar's receiver. In order to avoid ambiguity in the target range, the radar should transmit the pulse and specify adequate time for all echo signals to be received before the next pulse is generated. Otherwise, the received echo signal of the first transmitted pulse from a long-range target could be considered as the reflected version of the next transmitted pulse, which results in a wrong estimate of the target position. Thus, the longest range of interest determines the rate at which the pulses should be transmitted. This maximum unambiguous range (R_{un}) is given by [4]

$$R_{un} = \frac{c\,T_P}{2} = \frac{c}{2f_P} \tag{1.2}$$

where T_P is the pulse repetition period in seconds and f_P is the pulse repetition frequency in Hertz.

In radar systems, an RF signal is modulated and the task of the transmitter is to amplify the modulated RF signal to the desired level of transmission. The strong up-converted signal is then transmitted by the antenna to the surroundings. Depending on the transmitter architecture, a transmitter consists of a power amplifier to boost the RF signal, a mixer and local oscillator (LO) to modulate the signal (up-convert it to the desired frequency), filters to purify the spectrum and remove the unwanted frequency bands, and attenuators to decrease the power level in order to maintain the linearity of the system. The receiver also consists of several components such as a low noise amplifier (LNA) to amplify the weak received signal with a low contribution of added noise, filters and attenuators to perform the similar tasks of those in the transmitter chain, and a mixer to down-convert the signal to the baseband frequency [5].

In the receiver, the received modulated signal should be down-converted to a desired frequency depending on the receiver architecture by the use of a reference signal (LO). There are several receiver architectures such as super-heterodyne, zero-IF (direct conversion), and low-IF (intermediate frequency) conversion receivers. In super-heterodyne receivers, two down-conversion stages are used to convert the received high frequency signal into an IF signal and then convert the IF signal to the baseband signals through in-phase quadrature (I-Q) demodulators. Despite immunity to DC off-sets and high sensitivity (low input power and high output signal-to-noise ratio), the super-heterodyne architecture suffers from an image frequency component that falls relatively close to the desired frequency band and requires high-Q (quality factor) ceramic or surface acoustic wave (SAW) filters. Special image rejection mixing topologies such as the Hartley and Weaver architectures are employed in the literature to reject the unwanted image frequency of the super-heterodyne receivers. On the other hand, the zero-IF receiver has a simpler architecture in which the RF signal is directly converted into a baseband signal. However, this architecture also suffers from DC offset at the baseband and requires a high isolation in the mixers to avoid in-band interference. In order to overcome the image problem of super-heterodyne and the DC offset problem of zero-IF receivers, low-IF receivers are used in which the RF signal is down-converted to an IF signal in the range of several hundred kHz to several MHz [6]. Nevertheless, the low-IF receiver also suffers from image frequency and I/Q mismatch problems if proper frequency planning is not considered. Hence, the selection of receiver topology depends on the system requirements and the intended applications. In almost all radar systems, the receiver is a super-heterodyne architecture and the signal bandwidth is determined by the bandwidth of its IF stage [4]. In conventional radars, a matched filter is utilized whose impulse response is the time reversed transmitted signal [7]. Consequently, the bandwidth of the matched filter is proportional to the bandwidth of the transmitted signal, which adds to the design complexity if wideband signals are to be used.

Recently, digital receivers are being used instead of conventional ones. The difference between these two receivers is in the signal processing part where digital receivers employ analog-to-digital converters (ADCs) at the IF stage of the receiver. By using ADC, digital signal processing techniques such as digital filtering and adaptive beamforming could be implemented as well as other improvements such as higher flexibility, stability, and precision compared to analog receivers. Digital radars consist of both analog and digital components. In the receiver, the signal received by the antenna is down-converted to the IF stage through one or more down-converting mixer stages (analog part). Then the ADC directly samples the IF signal (IF sampling) to be processed in the digital domain and extracts the target information. It also provides storage and offline processing of data. With this method, the digital radar gains some advantages such as higher precision and stability, which are difficult to achieve with conventional analog receivers [8].

1.2 Digital Radar Systems

The main difference between analog and digital radar is in the receiver architecture. In digital receivers, the RF signal is down-converted to a lower frequency called IF which is then digitized by an ADC. This helps the receiver to retain all the information modulated into carrier frequency [9]. After digitizing, signal processing techniques such as digital filtering can be applied to the signal. Digital filters are of interest compared to their analog counterparts whose performance is degraded by low quality factor components.

Radar systems are desired to have high range resolution, high dynamic range, and multiple receiver channels. In the following section, the definition of each term is described, as well as the approaches that have been proposed or implemented in the literature on the design of radar.

1.3 High Range Resolution

High range resolution is the ability of a radar system to identify targets which are close to each other or to determine the profile of a large target. If a radar has low range resolution, it is not able to identify whether the scatterer originates from two closely spaced targets or one extended large target. When a signal is transmitted, the radar processes the echo reflecting back from the targets which could be defined as superposition of signals radiated from localized scattering centers on the target. High range resolution radars thus have the ability to scan smaller portions of the surroundings and get a better target profile. Range resolution of radar system is inversely proportional to the bandwidth of the transmitted waveform [10].

W-band frequency modulated continuous wave (FMCW) radar for "airborne situational awareness" is presented in [11]. A direct digital synthesizer (DDS) is used to generate a chirp for the transmitter rather than sending continuous pulses. Although FMCW requires high transmitter-to-receiver isolation and linear frequency sweep to avoid intermodulation (IMD) products, it has some advantages over pulsed waveform radars such as increased average power, narrowband IF processing, and suitability in short range applications. The transmitted FMCW signal is used as a LO in the receiver and is mixed with the reflected waveform from the target at the receiver and processed by a low pass filter (LPF) to eliminate the higher frequency component of the mixing product. The result is a tone whose frequency is proportional to the target range (R) in meters. The following relation is obtained:

$$\Delta R = {}^{c}/_{(2B)} \tag{1.3}$$

where ΔR is the range resolution (in meters), c is the speed of light ($3 \times 10^{8}\, {}^{m}/_{s}$), and B is the signal bandwidth (in Hz).

Equation (1.3) indicates that increasing the bandwidth of the transmitted signal improves the range resolution. As an application, a higher bandwidth of the transmitted signal is used to help pilots during landing in severe weather conditions such as the presence of fog, rain, snow, and smoke where the visual sight is limited. Hence, the radar is able to detect small obstacles in the landing zone of the plane by increasing the bandwidth which corresponds to improved range resolution.

1.4 High Dynamic Range

Dynamic range is a measure of the sensitivity level of the radar, i.e. the minimum detectable signal and strongest signal that can be received under linear conditions. Any signal less than the sensitivity level cannot be detected, while signals above the strongest signal would drive the system into nonlinearity and cause system saturation. It is important that naval radars which may operate in littoral regions have high dynamic range since high clutter reflections may mask a weak target. There are several definitions for dynamic range such as spurious free dynamic range (SFDR), 1 dB compression dynamic range (CDR), and ideal linear dynamic range (ILDR) [12]. For this study, SFDR is of interest.

1.5 Digital Radar Receivers Design Trade-off

1.5.1 Dynamic Range vs. Sensitivity

The trade-off between sensitivity and dynamic range in designing digital radar receivers is presented in [13]. This work simulates different scenarios that the designer faces and the compromise between sensitivity and dynamic range of the digital receiver. To have the highest sensitivity, "the overall gain of the RF front end should be as high as possible and the noise figure (NF) of the LNA should be as low as possible [13]." Since sensitivity is improved by detecting weaker signals and the overall NF of the receiver is dominated by the first element in the RF front end, an LNA with low noise contribution should be placed very close to the RF antenna. On the other hand, when the overall gain of the RF front end is very high and the utilized components are of low linearity, strong signals would saturate receiver blocks and drive them into nonlinearity. Hence, a designer should compromise between these two parameters based on the design requirements.

To have the largest dynamic range, "the gain of the RF front end should not be too high while the output P1dB compression point of the LNA should be as high as possible [13]." When the output P1dB compression point of the LNA is high enough, the LNA is not saturated by strong input signals. Consequently, the linearity range of the receiver is increased which results in an increase of the total dynamic range of the receiver as well. However, the SFDR does not only depend on the first RF front end block, but also on the other blocks such as nonlinear mixers, which adds IMD products to the RF spectrum. Thus, in order to have a high SFDR, the signal power level at the input of each block should be less than the specified input P1dB compression point and input third-order intercept point (IIP3) of the block. The linearity of all RF front end blocks should be maintained for different input signal power levels for which the receiver is designed. This will be discussed in more detail in the system development chapter of this thesis.

1.5.2 Dynamic Range vs. Noise Figure

Design trade-off for having high dynamic range with reasonable NF in digital receivers is also discussed in [14]. This work presents simulation results of an S-band digital receiver design on different aspects from point of view of ADC noise figure degradation, as well as maintaining the linearity margin of nonlinear blocks in the receiver. It compares the theoretical calculations of SFDR, CDR, and ILDR, cascaded system parameters such as cascaded gain and cascaded NF, and compares them with the simulation results obtained by Agilent's advanced design system (ADS) software. In order to reduce the ADC noise contribution (or the noise degradation due to ADC), the gain of RF front-end of digital radars should be as high as possible while its NF should be as low as possible. However, although the sensitivity of digital radars is improved by increasing the gain, the dynamic range of such systems is degraded due to the increase in the overall gain which drives the system into saturation. Another approach is to use a larger dynamic range ADC along with automatic gain control (AGC) at the receiver to improve the input sensitivity whenever necessary, without driving the system into nonlinearity for strong input signals [15].

To conclude, there is always a trade-off between the values of sensitivity, NF, gain, and the dynamic range of digital radar systems. Hence, the designer's task is to choose the optimal point based on the design requirements and the need of the intended application. In addition, the link budget and frequency plan of the system should be calculated to avoid system nonlinearity. This can be determined by considering the P1dB compression and IP3 points of individual blocks and choosing the gain of different stages to maintain a lower signal level at their inputs. The power levels of the signal at the input of each individual block should be less than the specified compression and IP3 to avoid system saturation by preventing the generation of nonlinearities in the system.

1.6 Digital Array Radar (DAR)

A digital array radar (DAR) is constructed by replication of a single digital receiver channel. In such radars, multiple receiver channels are used to construct multiple simultaneous beams (beamforming), based on the angle of arrival of the received signal at each channel in order to track a specific target in a certain direction and reject all other signals (due to jamming/interference, etc.) from other directions [16]. DAR utilizes ADC at the IF stage behind each receiver element, which improves the overall dynamic range of the receiver. However, to accommodate wider bandwidth for higher range resolution, the Nyquist theorem dictates that a high-speed ADC with a higher sampling frequency and higher number of bits is required. By increasing the bandwidth and utilizing a faster ADC, the overall dynamic range is reduced since the noise floor is increased. Hence, there is a trade-off between having high dynamic range and high bandwidth (i.e., high range resolution) in DAR. To overcome this dilemma, stretch processing provides a solution [17]. In this technique, two wideband signals are multiplied at the receiver and a tone proportional to the target range is generated. The stretch processing technique is discussed in the following section.

1.7 Stretch Processing in Radars

As stated earlier, range resolution is the ability of the radar to distinguish between two closely spaced targets. In order to have a high range resolution, wide-bandwidth signals are to be utilized in radar systems. However, in addition to a large amount of generated data, wide-bandwidth signals require high-speed ADC which introduces more noise to the system and degrades the overall dynamic range [18]. Hence, in conventional DAR with matched filtering, there is a trade-off between the high dynamic range and high range resolution (i.e., wide-bandwidth signal). To overcome this dilemma, stretch processing can be used [17]. Stretch processing helps digital radar to have reasonable bandwidth (i.e., high range resolution), while maintaining the requirements of using reasonable ADC speed. In this method, two linear frequency modulated (LFM) chirps with identical duration T are generated as transmitter "$S_{TX}(t)$" and local oscillator (LO) "$S_{LO}(t)$" waveforms. A guard time interval is added to the LO chirp in practice in order to ensure that the entire range window of interest is captured. Hence, prior knowledge about the range window of interest is necessary. The LO chirp is kept as the reference signal and is fed to the receiver LO port to down-convert the received chirp (a time-delayed version of the transmitted chirp).

$$S_{TX}(t) = \cos\left[2\pi\left({}^{k}/_{2}\, t^2 + f_{TX}^{(initial)} t\right)\right] \tag{1.4}$$

$$S_{LO}(t) = \cos\left[2\pi\left({}^{k}/_{2}\, t^2 + f_{LO}^{(initial)} t\right)\right] \tag{1.5}$$

where $f_{TX}^{(initial)}$ and $f_{LO}^{(initial)}$ are the transmitter and local oscillator initial frequencies, respectively, and k is the chirp rate which is the ratio of the chirp bandwidth to the chirp duration given by equation (1.6) below:

$$k = \frac{B}{T} \tag{1.6}$$

The transmitted signal is reflected in the presence of an object and received in the receiver after some time delay (τ). Depending on the time delay of the reflected signal, the LO chirp is then mixed with the received chirp "$S_{TX}(t-\tau)$" which is received in the receiver. The result of this mixing is the sum and difference of the input terms. The high frequency term which is a chirp can be filtered by a band pass filter (BPF), while the low frequency term is a tone whose frequency is given in equation (1.7) and contains the range profile of the targets.

$$k\tau + (f_{LO}^{(initial)} - f_{TX}^{(initial)}) \tag{1.7}$$

From equation (1.7) above, the resultant tone frequency is proportional to the time delay (τ) which indicates the dependency of the received signal's frequency on the target range. An important element in this process is the BPF which should be placed after the down-converter mixer. To pass the tone, the BPF should be centered at "$f_{LO}^{(initial)} - f_{TX}^{(initial)}$" and its pass band confined to the target range of interest and ADC capabilities. Thus, by limiting the target range of interest to a narrow frequency by stretch processing, wideband waveforms are processed as shown in Figure 1.2, without utilizing high-speed ADC. The resultant tone is digitized by ADC. Also, by applying the Fourier transform, the tone which corresponds to a certain target range profile is extracted. Hence, stretch processing is used to meet both requirements of high range resolution (having wide-bandwidth signals) along with using ADC with reasonable capabilities and sampling rates [19].

1.8 DAR Implementation in the Literature

1.8.1 DAR Testbeds

An S-band digital array radar testbed with 16 down conversion receivers is presented in [20]. Radars with low dynamic range cannot operate in cluttered environments such as coastline regions, and low instantaneous bandwidth decreases the range resolution of the radar. This can be improved by use of stretch processing, but still little is known about the actual performance of such processing with real radar data. The testbed is implemented by a single transmitter channel and 16 receiver channels. The transmitter is used in two modes: wideband and narrowband. In the wideband mode, an LFM pulse of 500 MHz is transmitted while in the narrowband mode, a 10 MHz LFM pulse is transmitted. These signals along with the LO are generated by an arbitrary waveform generator (AWG). The AWG output is centered at 50 MHz and it should be up-converted to S-band frequency. This is done through a set of frequency multipliers developed for the design. These frequency multipliers should have good amplitude flatness and produce low spurious products in the required bandwidth. Since multipliers produce IMD products which fall in the desired bandwidth, their number should be decreased. Hence, the up-converter presented in [17] which uses two up-converter stages is preferable since the AWG signal is centered at higher frequency which eliminates the need of having multiple frequency multipliers to generate a chirp in the S-band frequency.

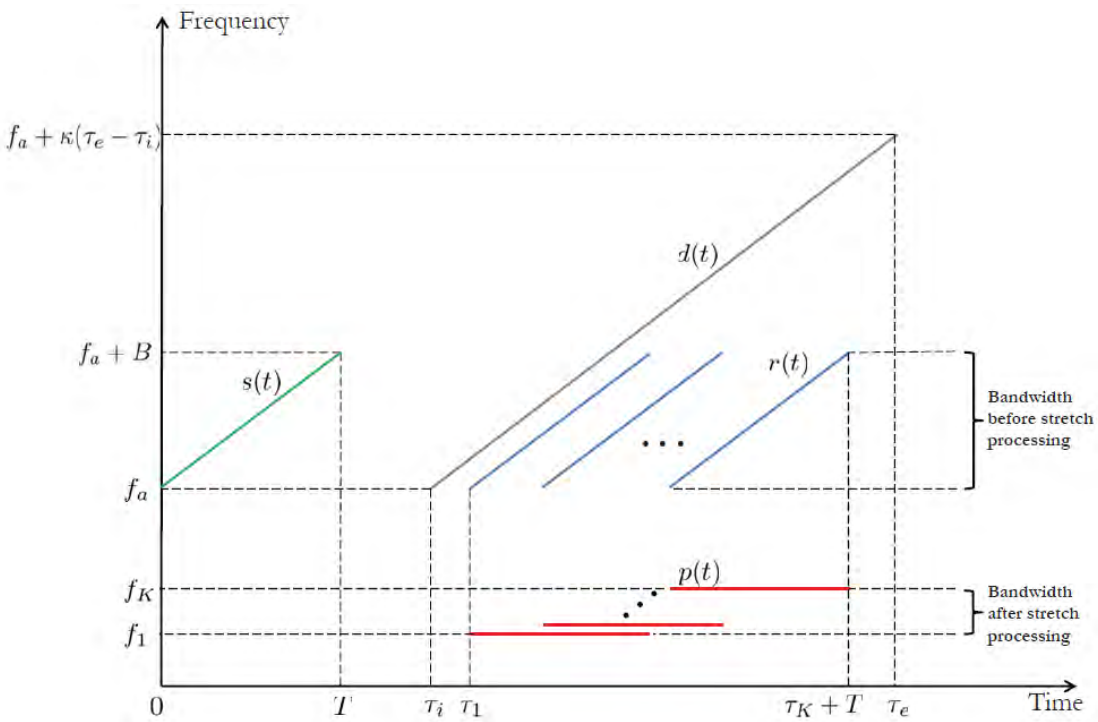


Figure 1.2: Stretch processing lineup [19].

The receivers consist of arrays of antennas which are located far from down-converters. The task of each down-converter is to shift the received S-band signal to an IF frequency of 70.5 MHz through two stages of analog mixers. The reason for using two-stage mixing is due to the large transmitted waveform bandwidth. In the wideband mode, since the transmitted waveform bandwidth is too large to be down-converted to IF frequency with a tone LO by the mixer, the LO is chosen to be an LFM signal as in stretch processing. The result of this down-conversion is a collection of IF tones whose frequencies are proportional to the delay of each target reflection. Then in the second mixer, the resultant tones are mixed with a fixed LO to down-convert the signal to an IF of 70.5 MHz and to be sampled by ADC. Using stretch processing, the available ADC can be used for higher bandwidth signals since the IF bandwidth is reduced. The data is then stored in a PC to be processed offline using MATLAB.

In down-conversion, the designer should be aware of the image frequency generated through the mixing process. An image frequency is a frequency which produces the same IF if mixed with LO. In [20], the first IF frequency is chosen so that the image frequency falls in the RF band where the filter's response shows a reasonable amount of attenuation. After digitizing the IF frequency, it is essential to equalize the pass band signal by removing the ripples added to it in the filtering and other stages. This is done through utilizing digital filters such as finite impulse response (FIR) filters. Additional equalization is required in the wideband mode where the LO is an LFM chirp. In this mode, the operation bandwidth is high and hence the variations in the RF front-end components are also increased which limits the adaptive beamforming.

1.8.2 PCB Implementations in the Literature

An S-band radar receiver array testbed is designed and implemented in [21]. An array of eight wide-band receiver channels is designed using commercial off-the-shelf (COTS) surface mount components assembled on two printed circuit boards (PCBs), each with four channel arrays. In the transmitter, a voltage controlled oscillator (VCO) is used to generate a 600 MHz LFMCW centered at 2.4 GHz. The voltage required by the VCO is supplied by a digital-to-analog converter (DAC) available on data acquisition (DAQ) device. A voltage adder is placed between the

DAC and VCO in order to adjust the output voltage level of the DAC to the input voltage requirement of the VCO to generate an LFM signal in the range of 2.1 – 2.4 GHz. The output of the VCO is filtered by an RF filter in order to remove the unwanted frequencies from the chirp. A power splitter is placed after the filter in order to split the chirp into two branches. One branch is passed through a power amplifier in order to transmit the chirp by antenna and the other branch is kept as a reference for feeding the receiver's LO. This reference LO is connected to the receiver to apply analog de-chirping in the receiver by down-converting the transmitted RF signal to a tone frequency which is proportional to the target range (stretch processing). Each receiver channel consists of an antenna which feeds the received RF chirp to an LPF with a cutoff frequency of 2.85 GHz. Then an LNA with 3 GHz bandwidth is placed to increase the power level of the received RF chirp. The RF chirp is de-chirped by the reference LO (sample of the transmitted signal) using I-Q demodulation. This converts the wide bandwidth chirp to baseband I-Q signals with very low bandwidth. The baseband signal is filtered by a fifth-order Butterworth LPF with a cutoff frequency of 31 kHz. Then, the I-Q signals are amplified by variable gain amplifiers and fed to the ADC for digitization. An important factor in designing this PCB is keeping the LO path equal in all receiver channels to avoid phase mismatch in the receiver arrays. Unfortunately, this work does not detail the design considerations and challenges faced to maintain system parameters such as linearity, dynamic range, gain, and NF.

1.9 Problem Statement and Methodology

Radar systems are characterized by different specifications such as dynamic range, range resolution, and number of receiver channels. A dual channel S-band digital radar testbed was designed and developed in [22] to meet the required specifications. This design utilizes large discrete microwave components which have good characteristics in the operating conditions. The aim of this thesis is to miniaturize the developed digital radar architecture while maintaining the same radar characteristics. This miniaturization is achieved by means of PCB level integration. However, the operating bandwidth of the surface mount components is limited and their performance at the PCB level is degraded as compared to discrete microwave components. Consequently, suitable COTS surface mount components are required and must be optimized to operate over the entire frequency band of interest. The impedance levels of different stages should be matched as well over the desired frequency bands to result in maximum power transfer of the signal in the system's chain. Furthermore, proper filters should be designed in order to maintain the system's linearity and reduce the overall cost of the radar system prototype. The unavoidable additional power loss in the PCB substrate in such transformations can be minimized by proper selection of the substrate material and circuit optimization.

It is desired to design a portable and miniaturized S-band radar system with high range resolution and high dynamic range at the PCB level. To increase the range resolution, the proposed design utilizes an LFM chirp as transmitting and receiving waveforms. On the other hand, for the radar system to operate in high clutter environments such as coastline regions, high dynamic range radar is of interest. However, it is difficult to maintain both requirements in the radar system simultaneously. Thus, stretch processing is utilized to transmit wider bandwidth waveforms and DAR with ADC behind each receiver channel to improve the overall dynamic range. The linearity of all stages of the radar system should be maintained and appropriate filtering should be considered to prevent the degradation of the dynamic range. Furthermore, by having multiple channel receivers, the radar system is able to form multiple beams simultaneously and use adaptive beamforming to track a target in a certain angular location and reject a jammer (spatial filtering).

1.10 Thesis Organization

The rest of this thesis is organized as follows. In Chapter 2, the novel radar testbed architecture and the system setup is introduced. In addition, Chapter 2 details the use of discrete microwave components in system implementation, alongside the development and simulation of the miniaturized radar system for PCB integration. Chapter 3 provides the design and full-wave EM simulation of different BPFs required for the miniaturized radar testbed on the PCB. Chapter 4 details the design, development, and simulation of the overall integrated radar system on the PCB. The test measurements versus simulation results of the fabricated radar testbed are compared in Chapter 5. The thesis is concluded in Chapter 6.

Chapter 2: Radar System Development and Simulation

The ultimate goal of this study is to design a high range resolution and high dynamic range radar system testbed on PCB. This reduces the physical size and the overall cost of the radar and enables its portability which it is useful in a variety of fields such as military applications. An S-band digital radar testbed was developed in [22] using discrete microwave components. A system architecture study and frequency plan were conducted focusing at selecting suitable COTS ICs in order to transfer the design to the PCB level using surface mount components. In the RF spreadsheet calculations, basic cascaded RF system performances such as cascaded gain, cascaded NF, cascaded IP3, and cascaded P1dB compression point were studied. The aim is to maintain the digital radar's specifications such as high dynamic range at the PCB level as well. However, the COTS surface mount components at high frequencies are of lower quality compared to discrete microwave components and the overall design is challenging. In this chapter, the details of the radar testbed architecture are introduced. Discrete microwave components were used to implement the radar testbed architecture in order to validate its functionality. The basic RF system definitions required for the frequency plan and the cascaded system calculations were derived from the literature. The frequency plan of the existing architecture was adopted in the new design; however, the cascaded system calculations were optimized to account for the new miniaturized system. Ultimately, the new design was simulated and the results were used to determine the validity of the initial cascaded calculations.

2.1 Digital Radar System Setup

Figure 2.1 depicts a high-level block diagram of a digital radar testbed. It is divided into four major sections:

1) The AWG which is used to generate the baseband chirps for the transmitter (TX) and local oscillator (LO) channels.

2) The up-converter which is used to shift the chirp generated by the AWG to the S-band and is divided into two channels: the TX channel for transmitting the

S-band chirp and the LO channel which is used as a reference for down-converting the chirp at the receivers (stretch processing).

3) An array of receivers which are used to shift the S-band chirp to an IF tone suitable to be digitized by ADC.

4) The ADC which digitizes the signal at the output of each receiver channel.

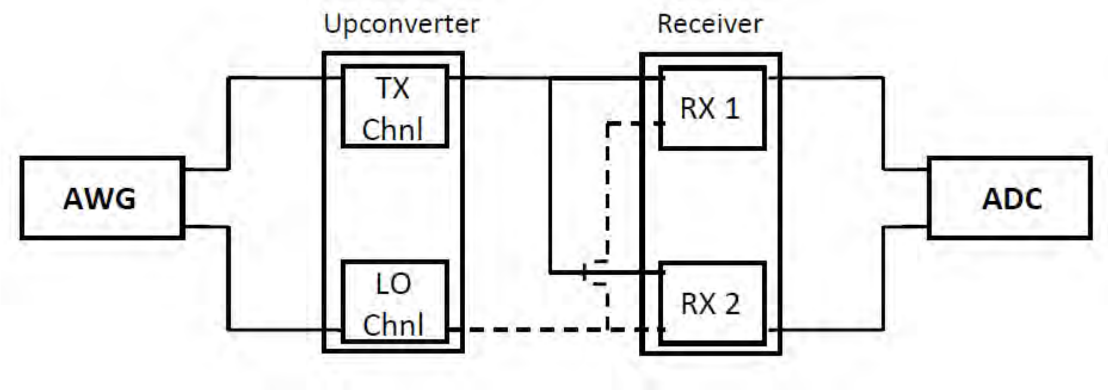


Figure 2.1: Block diagram of digital radar testbed.

2.1.1 Up-converter

In order to shift the generated baseband chirp to the S-band, mixers should be used. However, mixers introduce IMD products which usually fall in the frequency band of interest and are difficult to filter. If the IMD products are strong enough, they may drive the system into nonlinearity which corrupts the signal, thus reducing the overall dynamic range. These IMD products should be considered in the design and the frequency plan should be taken into account in order to reduce their power by appropriate filtering. Hence, after the mixer, a BPF is used in order to pass the desired frequency band and reject other out-of-band frequency components. To avoid strong in-band IMD products, the up-converter utilizes two stages of up-conversion through the use of a mixer and a frequency doubler.

The amplifiers and attenuators (PAD) are used at some stages in order to tune the power level of in-band signals in order to maintain the linearity of the system. The power level at the input of each block should be less than the block P1dB compression point to ensure block linearity. Figure 2.2 and Figure 2.3 show the TX and LO channel architectures, respectively. The inputs of these channels are fed by the AWG, which generates a 100 μs LFM chirp of 300 MHz instantaneous bandwidth with 350 MHz center frequency (200-500 MHz) and a power level of 0 dBm. The frequency versus time response of this generated baseband chirp along with its frequency spectrum are shown in Figure 2.4. The chirp power is calculated by the integration of the area under its spectrum curve.

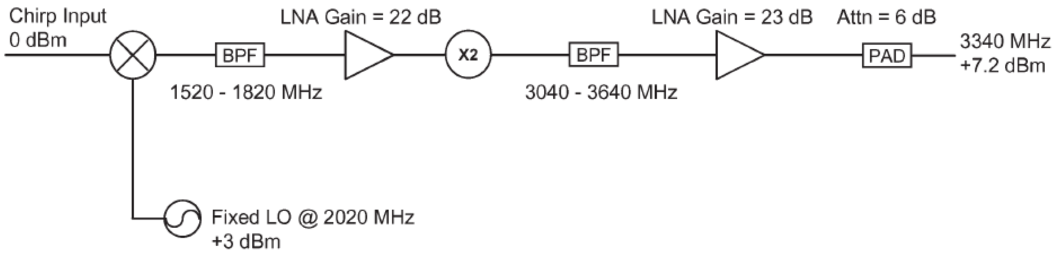


Figure 2.2: Up-converter block diagram (TX channel) [22].

In the first up-conversion stage, the LFM chirp is mixed with an oscillator with a power level of 3 dBm at 2.02 GHz and the difference frequencies (lower side band) are passed by a BPF. The LNA is used to increase the power level of the signal at the input of the frequency doubler to a level suitable to drive this passive component. After the doubler, the instantaneous bandwidth of the chirp is increased to 600 MHz which is adequate for the desired range resolution of the system as shown in equation (1.3) of Section 1.3.

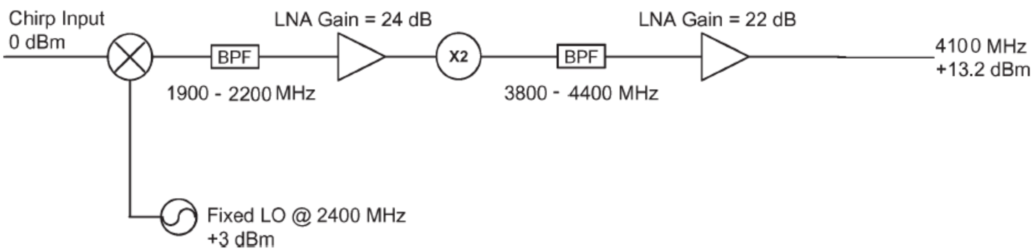
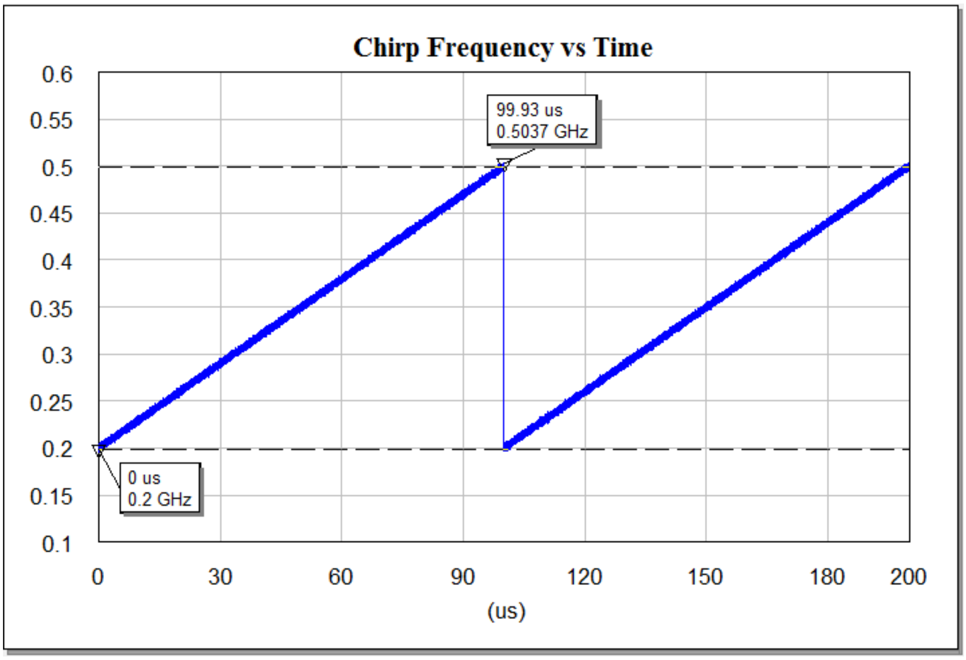


Figure 2.3. Up-converter block diagram (LO channel) [22].

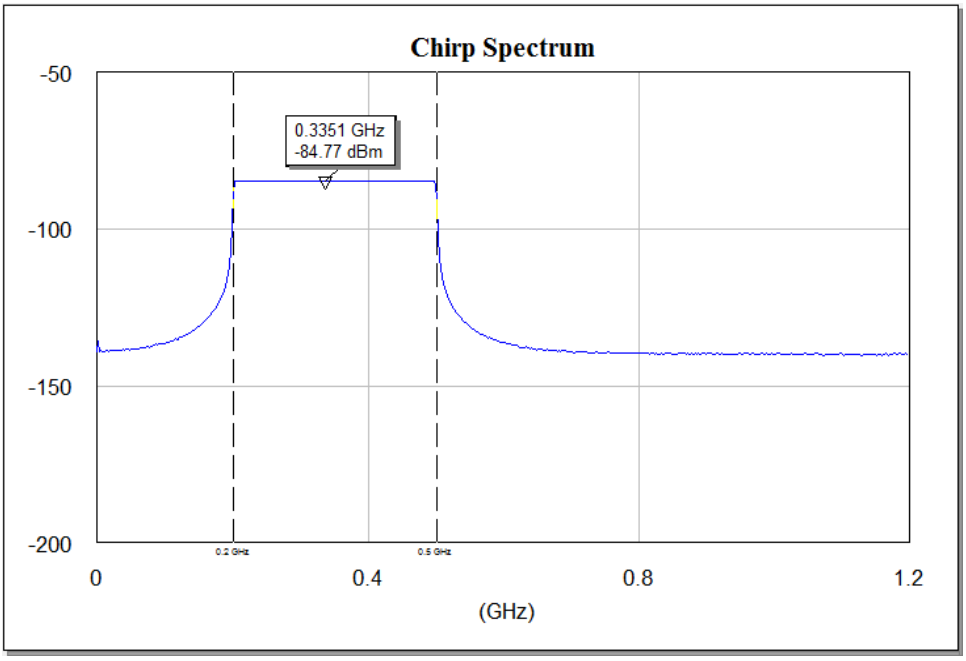
The LO channel consists of stages identical to the TX channel except for the difference in the frequency of operation. This difference in frequency is set to 760 MHz due to the requirement of some surveillance radar systems [22]. The output of the TX channel is a chirp with 3040-3640 MHz bandwidth (3340 MHz center frequency) with a power level of 7.2 dBm and the output of the LO channel is a chirp with 3800-4400 MHz bandwidth (4100 MHz center frequency) with a power level of 13.2 dBm. The output of the TX channel is transmitted while the output of the LO channel is fed to the receivers for stretch processing.

2.1.2 Receiver

The receiver architecture is a super-heterodyne receiver which consists of two down-conversion stages. In the receiver (RX), the TX and LO channels are mixed using stretch processing and the lower side-band frequency, which is a tone proportional to the target range, is passed by a BPF. The attenuator and LNA are used to shift the power level of the signal to avoid nonlinearity. In order to get the 70 MHz baseband signal to be sampled by the ADC, the signal is down-converted by an 830 MHz oscillator. The two-stage down-conversion helps in rejecting the image frequency. The 16 MHz BPF is an important component since its pass band is proportional to the range of interest of the target profile (see Section 1.7 on stretch processing). The power level of the output signal of the RX channel is fixed at 4 dBm by the final LNA and PAD in the RX chain. The block diagram of each receiver channel is shown in Figure 2.5.



(a)



(b)

Figure 2.4: Baseband chirp (a) Frequency vs. time (b) Spectrum.

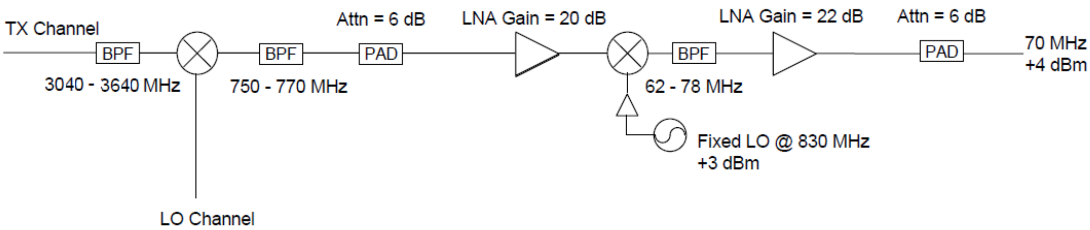


Figure 2.5: Receiver block diagram (RX channel) [22].

2.2 Digital Radar Testbed using Discrete Microwave Components

The radar system was implemented using discrete microwave components. Figure 2.6 shows the constructed radar system in the lab. As labeled in the figure, the radar testbed consists of TX and LO channels in addition to two RX channels. The implemented system is bulky due to the use of large scale components.

Figure 2.7 represents the output of the first RX channel when the specified chirp was applied to the system. The output of the receiver is a strong tone at 70 MHz which corresponds to the range profile of the target. The pass band of the last BPF (62-78 MHz) is observed on the output spectrum as well. The output spectrum indicates 60 dB and 90 dB of in-band and out-of-band dynamic range, respectively.

The achieved high dynamic range verifies the linearity of the overall system and indicates the validity of the proposed digital radar's architecture.

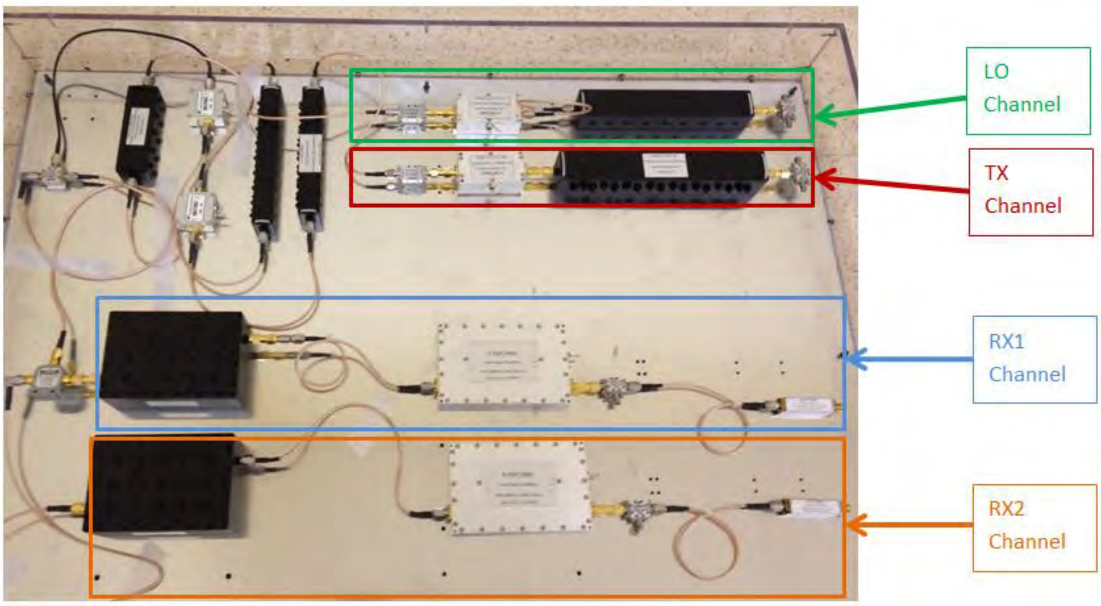


Figure 2.6: Digital radar testbed using discrete microwave components.

2.3 Basic RF System Concepts

In the following section, the necessary terminologies for the spreadsheet calculations of RF systems and the associated cascaded formulas are provided.

2.3.1 Cascaded Gain

Whether each block in a system is active or passive, the block increases or decreases the power level of its input signal, respectively. The active element can increase the signal power level by having a positive gain whereas passive elements reduce the signal power level by having a negative gain or attenuation. The cascaded gain of cascaded stages is obtained by linear multiplication of the gain of the individual stages. The cascaded gain calculations are easier when the individual gains are converted to dB where they are found by the summation of the power gain of each cascaded stage. Equation (2.1) represents the overall cascaded gain of a system where i is the index of each stage, N is the number of the cascaded stages, and G is the gain of the individual stage in dB.

$$G_{cascaded} = \sum_{i=1}^{N} G_i \tag{2.1}$$

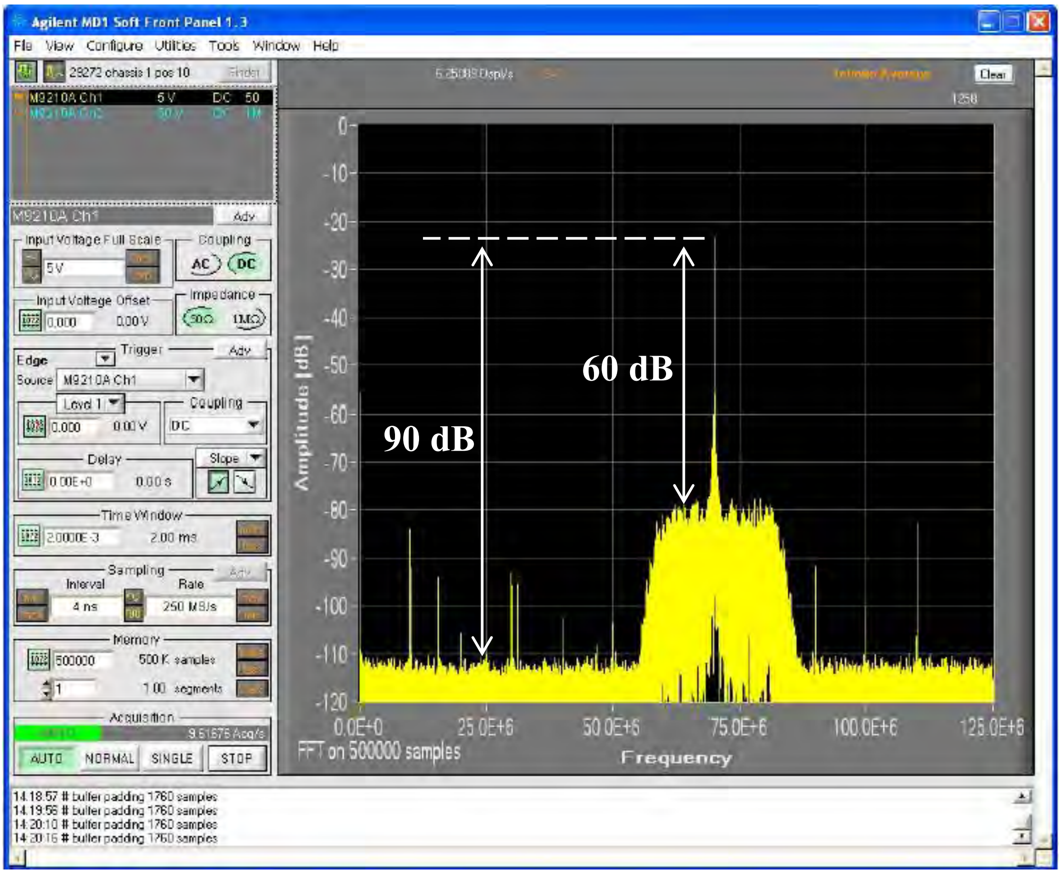


Figure 2.7: Digital radar testbed output of discrete microwave components for LFM chirp input (200-500 MHz); 600 MHz instantaneous bandwidth.

2.3.2 Cascaded NF and SNR

The noise factor of an electronic circuitry defines the noise contribution of the circuit to the input signal. In other words, the noise factor is a measure of the added noise to the original signal when passed by the electronic block (circuit). The noise factor of a circuit is measured by the ratio of the input SNR_i over the output SNR_o. Equation (2.2) provides different formulas for noise factor calculation where the noise is defined by the symbol N [23].

$$f = \frac{SNR_i}{SNR_o} = \frac{N_{o(total)}}{G\ N_{i(source)}} = 1 + \frac{N_{o(added)}}{N_{o(source)}} \tag{2.2}$$

Equation (2.2) shows that for a noiseless circuit, the noise factor equals 1. However, such an ideal circuit is not achievable in practical scenarios. The cascaded noise factor is of interest in order to specify the degradation of SNR through the system. The noise factor of the *N*-stage cascaded system is defined by [12]:

$$f_N(Linear) = f_1 + \frac{f_2 - 1}{G_1} + \frac{f_3 - 1}{G_1 G_2} + \cdots + \frac{f_N - 1}{G_1 G_2 . \dots . G_{N-1}} \tag{2.3}$$

where G_i and f_i are the linear gain and noise factor of each stage, respectively. As seen from equation (2.3), the cascaded noise factor of a system is mainly affected by the noise factor of the first stage. Hence, LNAs are used in most communication systems to reduce the overall noise factor of the system and increase the SNR. Equation (2.4) relates the noise factor of individual or cascaded stages to the individual or cascaded NF in dB, as

$$NF = 10 \log_{10} F \tag{2.4}$$

2.3.3 Cascaded IP3

IMDs are generated in the system due to nonlinear blocks such as mixers or when a linear block such as an amplifier is driven to the saturation level. The generation slope of the third-order products is steeper than the second-order products due to their cubic nonlinearities rather than square ones. Hence, IP3 is a measure of the linearity in a cascaded system and determines the IM distortion. IP3 is a theoretical point where the powers of the desired (fundamental) signal and the third-order distortion (IMD3) are equal [24]. The graphical illustration of IP3 is shown in Figure 2.8. From this figure, the output IP3 (OIP3) is higher than the input IP3 (IIP3) of the linear gain, as the theoretical intercept point lies on the linear response curve:

$$IIP3\ (dBm) = OIP3(dBm) - Gain(dB) \tag{2.5}$$

Equation (2.6) below relates the linear ip3 to the IP3 in dBm scale.

$$IP3(dBm) = 10 \log(ip3) \tag{2.6}$$

In order to calculate the linear IIP3 (in mw) of an *N*-stage cascaded system, equation (2.7) is used [24]:

$$iip3_N(Linear) = \frac{1}{\frac{1}{iip3_1} + \frac{1}{iip3_2} + \cdots + \frac{1}{iip3_N}} \tag{2.7}$$

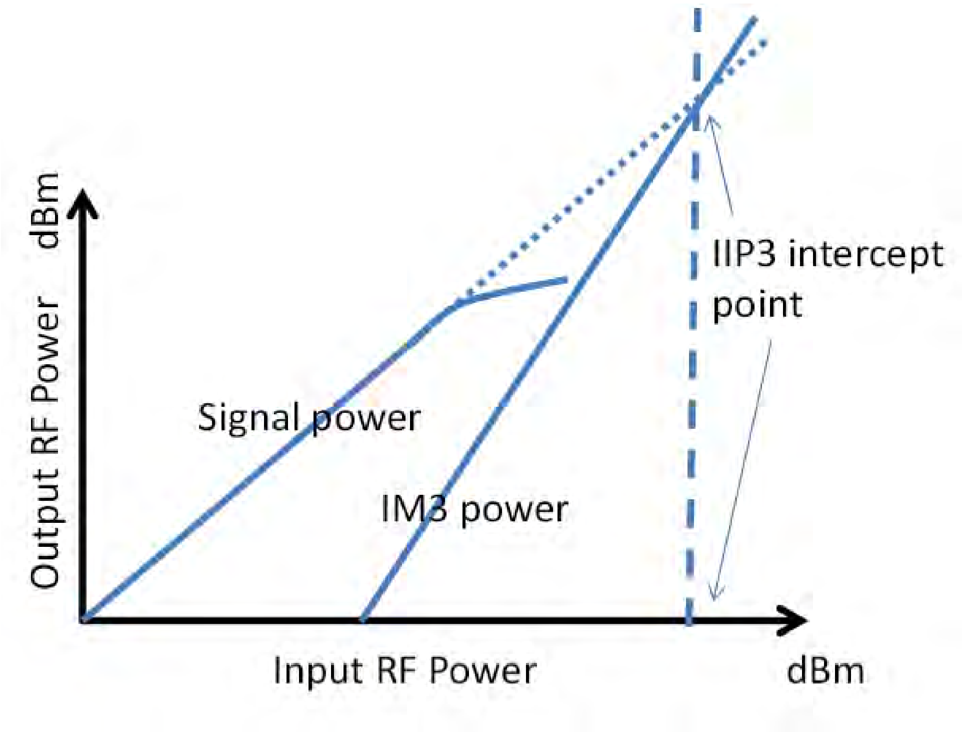


Figure 2.8: Intercept point definition.

2.3.4 Cascaded P1dB Compression Point

Another measure of the linearity of a cascaded system is the P1dB compression point. The P1dB compression point is defined as the point at which the gain of a circuit is reduced by 1 dB due to overdrive or saturation, as shown in Figure 2.9.

Hence, the relation between the output and input P1dB compression points is given by equation (2.8) below.

$$P1dB_{input}(dBm) = OP1dB\ (dBm) - (Gain\ (dB) - 1) \tag{2.8}$$

In order to maintain the linearity of electronic circuitry, the signal power at its input should be less than the input P1dB compression point. As a rule of thumb, the P1dB compression point occurs at 10-12 dB below the intercept point of the device

[24]. Equation (2.9) defines the relation between the P1dB compression points in dBm and linear (p1dB) scales.

$$P1dB\ (dBm) = 10\log(p1dB) \tag{2.9}$$

The OP1dB compression point of two cascaded stages is given by:

$$op1dB_N(Linear) = \frac{1}{\frac{1}{op1dB_{n-1} * G_n} + \frac{1}{op1dB_n}} \tag{2.10}$$

where n is the current stage and n-1 is the previous stage components. This equation can be extended to find the cascaded OP1dB compression point of the overall system. Consequently, equation (2.8) along with the cascaded gain of the system can be used to transform the obtained cascaded OP1dB into the cascaded input P1dB. The cascaded input P1dB defines the maximum input power which causes nonlinearity and drives the system into saturation.

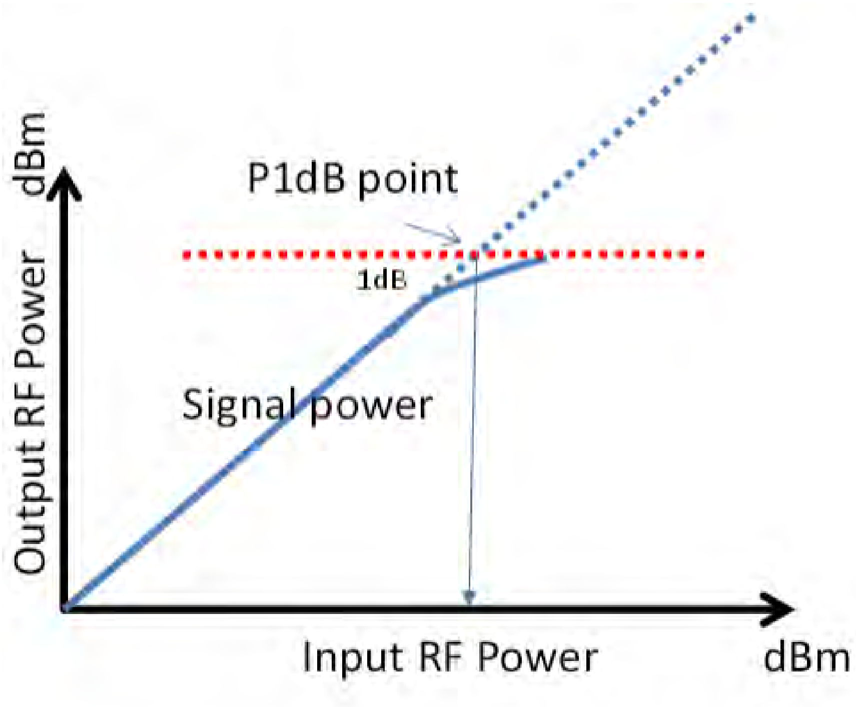


Figure 2.9: P1dB compression point definition.

2.4 Digital Radar Development for PCB Integration

In order to develop the miniaturized radar system at the PCB level, the first step was to check the availability of the required surface mount components in different IC manufacturer catalogs. For the PCB level, the functionality of the selected surface mount components should be stable over the wide range of frequency bands of interest, as a wideband chirp signal was used in the radar system architecture. In addition, the impedance level of these devices over the entire frequency band is an important factor in such selection. Hence, some difficulties were faced at this stage to seek the best IC components for different stages. After the IC selections, the next step was the spreadsheet analysis for the new cascaded RF system to estimate the cascaded system parameters and anticipate a proper link budget which suited the specifications and requirements of the selected components. Consequently, the system was simulated using the RF budget simulation tool in ADS software to verify the spreadsheet calculations. Then, the visual system simulator (VSS) in AWR software was used to verify the overall system parameters and test the system linearity for wideband chirp signal excitation.

2.4.1 Spreadsheet Calculation versus ADS RF Budget Simulation

To verify the effect of individual blocks on the overall system parameters, cascaded analysis was performed. For each channel of the digital radar system, the cascaded analysis was done in spreadsheets using the cascaded RF system equations presented in Section 2.3. The results of the obtained parameters from these calculations in addition to the ADS simulation results of each channel are provided in the following section.

2.4.1.1 TX and LO channels

Table 2.1 and Table 2.2 represent the spreadsheet analysis of the TX and LO channels along with the associated ADS simulation results, respectively. The spreadsheet analysis, which was created using Microsoft Excel, represents the selected surface mount component's models along with their individual parameters such as gain, NF, IP3, and P1dB compression points at the intended frequency of operation. These specifications are extracted from the component's datasheets provided by the manufacturers. The results of the cascaded calculations such as cascaded gain, cascaded NF, cascaded IP3, and cascaded P1dB compression point are also presented. Other concerns such as maintaining the linearity of each block in the system by comparing its specifications with the input signal levels are visualized in the spreadsheet calculations as well. Note that IP3 and P1dB are valid for components such as amplifiers and mixers. These values are considered to be high enough in passive components such as filters and attenuators and an ideal value of 1000 dBm (from ADS software) is considered in the calculations.

Table 2.1: PCB TX channel spreadsheet calculations vs. ADS simulation results.

Component		Mixer	BPF	Amplifier	Doubler	BPF	Amplifier	PAD	ADS Simulation
Part Number		T3-04	1520-1820 MHz	ADL5602	D-1505	3040-3640 MHz	MGA30789		Last Stage
Block Gain	dB	-7	-1	19.5	-10	-1	11.7	-5	-
Block NF	dB	7	1	3.3	10	1	3.8	5	-
Block IIP3	dBm	25	1001	22.5	20	1001	30.1	1005	-
Block OIP3	dBm	18	1000	42.0	18	1000	41.8	1000	-
Input 1 dB	dBm	12	1002	0.8	23	1002	13.8	1006	-
Output 1 dB	dBm	4	1000	19.3	12	1000	24.5	1000	-
Cascaded Gain	dB	-7.000	-8.000	11.500	1.500	0.500	12.200	7.200	6.945
Cascaded NF	dB	7.000	8.000	11.300	11.500	11.556	11.912	11.949	16.717
Signal Power at Block Input	dBm	0.000	-7.000	-8.000	11.500	1.500	0.500	12.200	-
Signal Power at Block Output	dBm	-7.000	-8.000	11.500	1.500	0.500	12.200	7.200	6.945
Cascaded OIP3	dBm	18.000	17.000	35.422	17.277	16.277	27.801	22.801	22.801
Cascaded IIP3	dBm	25.000	25.000	23.922	15.777	15.777	15.601	15.601	-
Cascaded O P1dB	dBm	4.000	3.000	17.601	6.256	5.256	16.252	11.252	11.606
Cascaded I P1dB	dBm	12.000	12.000	7.101	5.756	5.756	5.052	5.052	-

As it is seen in the TX spreadsheet, the input signal is considered to have a power level of 0 dBm. The signal power at the input of each block is maintained to be less than the specified input P1dB compression of that block to avoid nonlinearity and saturation. The cascaded gain is 7.2 dB which is close to the simulation result of 6.945 dB. The cascaded NF is expected to be high as the first component in the RF chain is the passive mixer with high NF. As discussed in Section 2.3.2, the first element of the cascaded RF system mostly affects the value of the cascaded NF (refer to equation (2.3)) and an LNA or a block with lower NF should be placed in the front end. However, maintaining a high power level of the wanted signal by having a reasonable SNR and avoiding the generation of IMDs or proper filtering of IMDs is significant in the overall system design. The large difference between the calculated NF of 11.949 dB and the obtained NF of 16.717 dB from ADS simulation is due to the presence of the mixer. ADS is considering single side band (SSB) noise in the mixer assuming the image frequency is filtered. However, in the spreadsheet calculation, double side band (DSB) noise is considered since the high-side band is not filtered before the mixer. The cascaded output IP3 obtained from spreadsheet calculation and ADS simulation has exactly the same value of 22.801 dBm and is greater than cascaded output P1dB compression. If the system input IP3 is greater than the input P1dB point, it is guaranteed that any input signal power which does not drive the system into saturation (below the 1dB compression point) will not produce significant high level IMDs. The same discussion of the TX channel is applicable for the LO channel specifications as well.

Table 2.2: PCB LO channel spreadsheet calculations vs. ADS simulation results.

Component		Mixer	BPF	Amplifier	Doubler	BPF	Amplifier	Amplifier	ADS Simulation
Part Number		T3-04	1900-2200 MHz	ADL5602	D-1505	3800-4400 MHz	MGA30789	MGA30789	Last Stage
Block Gain	dB	-7	-1	19.3	-10	-1	10	10	-
Block NF	dB	7	1	3.3	10	1	3	3	-
Block IIP3	dBm	25	1001	22.7	20	1001	30	30	-
Block OIP3	dBm	18	1000	42.0	18	1000	40	40	-
Input 1 dB	dBm	12	1002	1.0	23	1002	16.5	16.5	-
Output 1 dB	dBm	4	1000	19.3	12	1000	25.5	25.5	-
Cascaded Gain	dB	-7.000	-8.000	11.300	1.300	0.300	10.300	20.300	19.938
Cascaded NF	dB	7.000	8.000	11.300	11.510	11.568	11.841	11.867	16.668
Signal Power at Block Input	dBm	0.000	-7.000	-8.000	11.300	1.300	0.300	10.300	-
Signal Power at Block Output	dBm	-7.000	-8.000	11.300	1.300	0.300	10.300	20.300	19.938
Cascaded OIP3	dBm	18.000	17.000	35.265	17.253	16.253	26.073	34.597	34.597
Cascaded IIP3	dBm	25.000	25.000	23.965	15.953	15.953	15.773	14.297	-
Cascaded O P1dB	dBm	4.000	3.000	17.536	6.207	5.207	14.819	22.136	23.238
Cascaded I P1dB	dBm	12.000	12.000	7.236	5.907	5.907	5.519	2.836	-

Since the utilized frequency doubler is passive, it requires a minimum power of 10 dBm as a suitable driver input power. The lineup of TX and LO channels are designed such that the power level of the signal at the input of the doubler is greater than the required minimum power level. The utilized mixer is also a passive component and requires a minimum LO drive of 15 dBm. Except for the first mixer of the RX channel, the LO drives of all other mixers are provided by external oscillators. Since the output of the LO channel is kept as a reference and is fed to the receiver for down-converting the received signal (stretch processing), it should maintain the required minimum power level needed to drive the mixer. Hence, two amplifiers are cascaded at the last stage of the LO channel in order to increase its output signal power up to 20.3 dBm which satisfies the required mixer drive level while maintaining the linearity of the LO channel.

2.4.1.2 RX channel

The spreadsheet calculations and ADS simulation are performed for the RX channel as well. The output signal from the TX channel is the input to the receiver. From Table 2.3, the calculated cascaded gain is 7 dB which is close to the ADS simulation result of 6.657 dB. Similar to the previous channels, the high cascaded NF is expected as the mixer is used as the first element of the receiver's front end. However, maintaining a high power level of the wanted signal by having a reasonable SNR and avoiding the generation of IMDs/ensuring the proper filtering of IMDs is significant in the overall system design. The spreadsheet calculations show the output SNR of the receiver to be 90.91 dB which is close to the obtained result of 86.19 dB from the ADS simulation. Figure 2.10 shows the SNR trend at the output of each stage of the receiver obtained from the ADS simulation.

Table 2.3: PCB RX channel spreadsheet calculations vs. ADS simulation results.

Component		BPF	Mixer	BPF	PAD	Amplifier	Mixer	BPF	Amplifier	ADS Simulation
Part Number		3040-3640 MHz	T3-05	750-770 MHz		MGA-82563	T3-05	62-78 MHz	SBB1089Z	Last Stage
Block Gain	dB	-1	-7	-1	-6	14.5	-7	-1	15.5	-
Block NF	dB	1	7	1	6	2.2	7	1	3.3	-
Block IIP3	dBm	1001	25	1001	1006	16.5	25	1001	26.5	-
Block OIP3	dBm	1000	18	1000	1000	31	18	1000	42	-
Input 1 dB	dBm	1002	12	1002	1007	3.8	12	1002	4.5	-
Output 1 dB	dBm	1000	4	1000	1000	17.3	4	1000	19	-
Cascaded Gain	dB	-1	-8	-9	-15	-0.5	-7.5	-8.5	7	6.657
Cascaded NF	dB	1	8	9	15	17.2	17.557	17.667	18.228	22.696
Cascaded SNR at Block Output	dB	108.136	101.136	100.136	94.136	91.936	91.579	91.469	90.908	-
Signal Power at Block Input	dBm	7.2	6.2	-0.8	-1.8	-7.8	6.7	-0.3	-1.3	7.2
Signal Power at Block Output	dBm	6.2	-0.8	-1.8	-7.8	6.7	-0.3	-1.3	14.2	13.857
Cascaded OIP3	dBm	1000	18	17	11	24.422	14.691	13.691	28.969	28.969
Cascaded IIP3	dBm	1001	26	26	26	24.922	22.191	22.191	21.969	-
Cascaded O P1dB	dBm	1000	4	3	-3	10.486	0.725	-0.275	13.704	17.169
Cascaded I P1dB	dBm	1002	13	13	13	11.986	9.225	9.225	7.704	-

		Theoritical Value	ADS System Simulation
Input Signal Power	dBm	7.2	7.2
Input Noise Floor	dBm	-101.936	-101.704
Input SNR	dB	109.136	-
Output Signal Power	dBm	14.200	13.857
Output Noise Power	dBm	-76.708	-72.329
Output SNR	dBm	90.908	86.186
IIP3 referred to input	dBm	21.969	-
Sensitivity	dBm	-83.708	-
Dynamic Range (In band)	dB	70.452	67.532

Similar to the TX and LO channels, the difference between the calculated NF of 18.228 dB and NF of 22.696 dB obtained from the ADS simulation is due to the presence of mixers. In ADS, SSB noise is considered for the mixers, assuming that the image frequency is filtered. In the spreadsheet calculation, DSB noise is considered as the high side-band is not filtered before the mixer. The same value of 28.969 dBm is obtained for the cascaded output IP3 from both the spreadsheet calculation and ADS simulation. The obtained value is greater than the cascaded output P1dB compression which indicates less significance of the produced IMDs if signals with lower power levels are used at the input of individual blocks. However, IMDs cannot be avoided completely in any design and should be filtered effectively to avoid signal corruption.

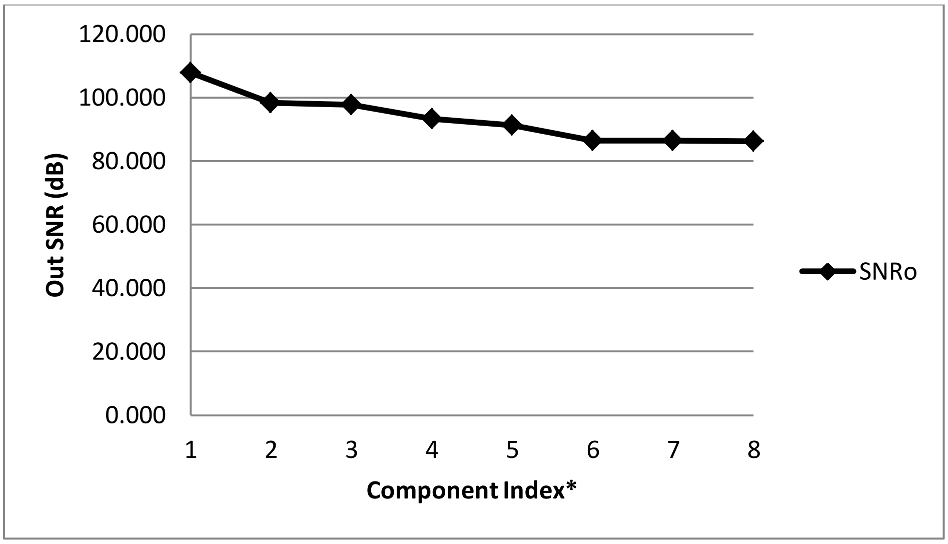


Figure 2.10: SNR at output of RX stages.

* Component index defines the number of each cascaded stage in the receiver chain

Receiver sensitivity is an important parameter which indicates the minimum signal power that the receiver is able to detect. Equation (2.11) below represents the receiver's sensitivity [12].

$$sensitivity = kTB + NF + SNR\ (wanted) \tag{2.11}$$

where k is Boltzmann's constant ($1.38 \times 10^{-23}\ J/K$), T is the absolute temperature (in kelvin), and B is the spectrum bandwidth (in Hz).

If the wanted SNR is not specified, the minimum detectable signal (MDS) is obtained by equation (2.12) below:

$$MDS = kTB + NF \tag{2.12}$$

The SFDR is the difference between the strongest input signal that the receiver can receive without distortion and the minimum detectable signal. The strongest signal is considered an input signal which creates IMD products equal to the wanted signal at the fundamental frequency. In theory, this signal is equal to the cascaded IIP3 of the receiver while the minimum detectable signal is obtained by equation (2.12) above. The SFDR is then obtained using equation (2.13).

$$SFDR = \frac{2}{3}(IIP3\ (dBm) - MDS\ (dBm)) \tag{2.13}$$

From Table 2.3, the calculated in-band SFDR is 70.452 dB while the ADS simulation shows an SFDR of 67.532 dB. Both values are close enough confirming that the desired high in-band dynamic range is achieved for the miniaturized radar testbed on the PCB.

2.4.2 AWR System Simulation

To verify the output spectrum of each channel, the system is simulated in AWR. The TX, LO, and RX channels are connected together to check the overall response of the system. The system is examined under two scenarios for single tone and wideband LFM chirp excitations.

2.4.2.1 Single tone input signal

As a preliminary simulation, a 350 MHz tone with 0 dBm power level was applied to both the TX and LO channels. Figure 2.11 and Figure 2.12 represent the output spectrum of the TX and LO channels, respectively. As labeled on the graphs, the output of the TX channel is a tone at 3.34 GHz with a power level of 7.047 dBm whereas the output of the LO channel is a tone at 4.1 GHz with a power level of 20.04 dBm. These results verify the spreadsheet calculations and ADS simulation of both channels. The spectrum of both channels is showing a peak signal, which is the desired signal, and other acceptable low amplitude harmonics. Hence, this is an indicator of reasonable filtering in both the TX and LO channels.

The generated signals for the TX and LO channels were applied to the receiver to verify the receiver's response in terms of linearity, gain, and dynamic range. Consequently, Figure 2.13 shows the receiver's output spectrum. As labeled on the graph, the RX output is a strong tone at 70 MHz with a power level of 13.52 dBm. The spectrum is indicating the generated harmonics of the fundamental frequency. However, the difference in the power levels of the fundamental frequency component at 70 MHz and the harmonics is high enough, which validates the undertaken system's frequency plan.

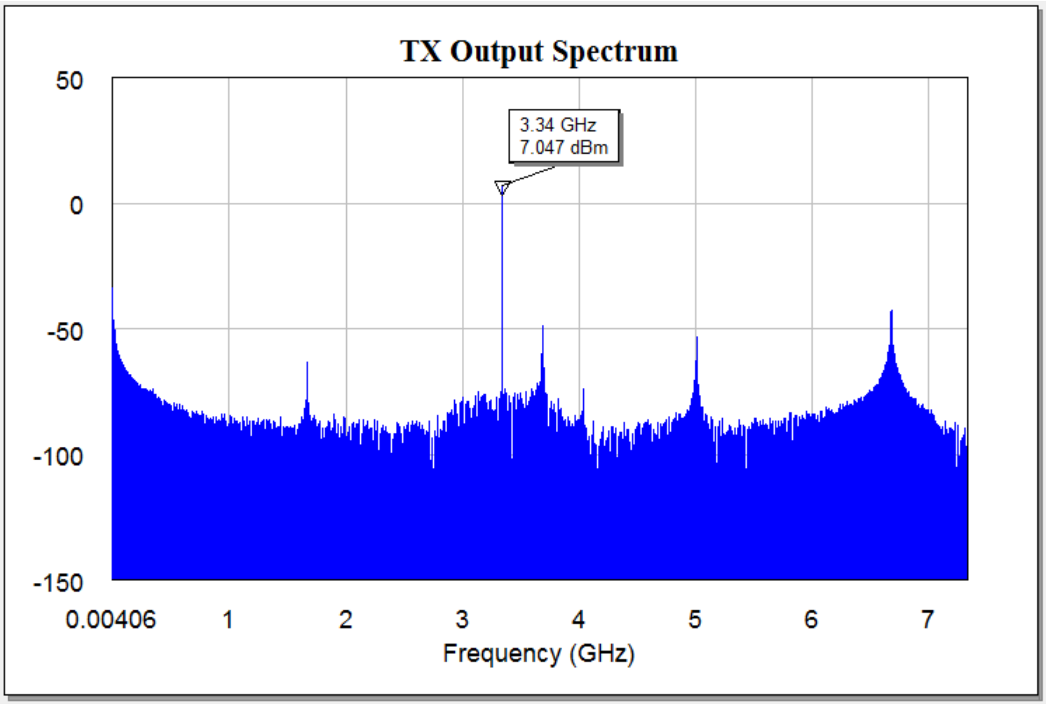


Figure 2.11: Output spectrum of TX channel for single tone input signal.

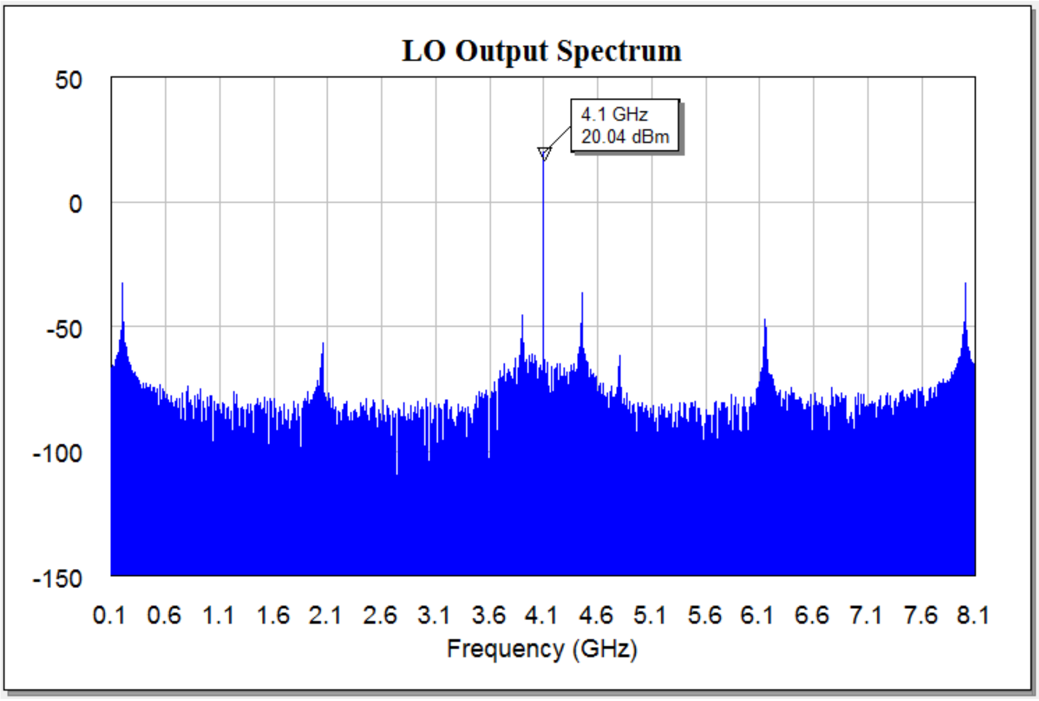


Figure 2.12: Output spectrum of LO channel for single tone input signal.

It is noted that using AWR simulation, the signal flow at different stages of the system was monitored to determine whether the block is operating under linear conditions or is driven into saturation. It was realized that if the block is driven into saturation, significant IMDs are generated at the output which reduce the output's dynamic range.

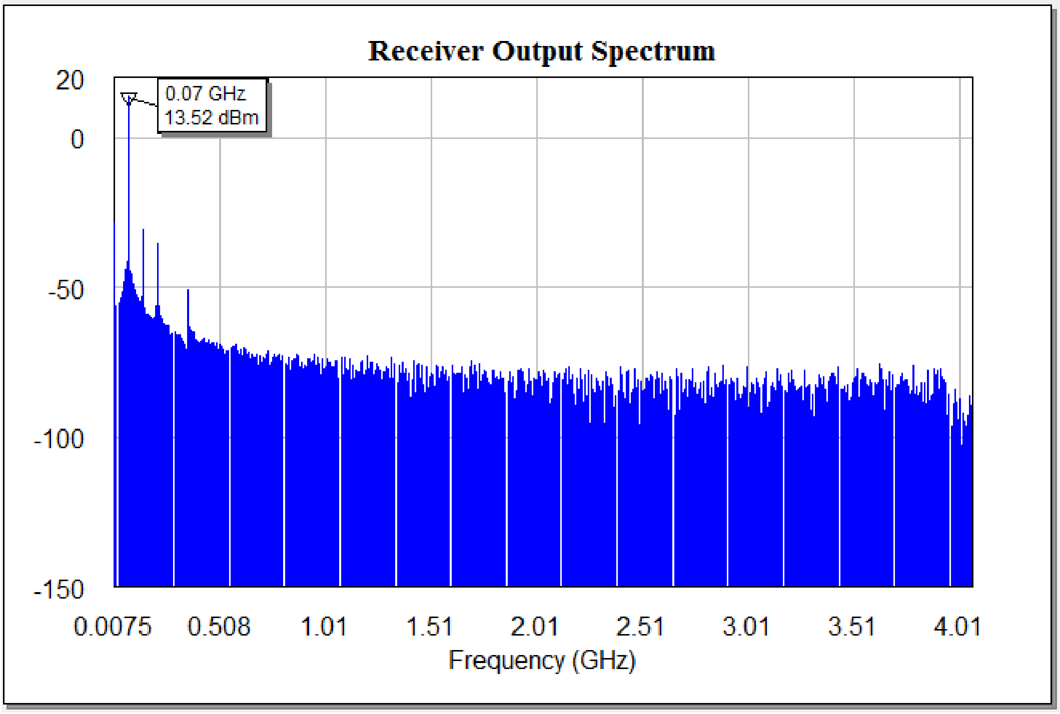


Figure 2.13: Output spectrum of RX channel for single tone input signal.

2.4.2.2 Wideband input signal (LFM chirp)

The overall functionality of the miniaturized digital radar system for PCB integration was examined by applying a 300 MHz baseband LFM chirp (200-500 MHz) at the inputs of the TX and LO channels. Hence, the overall linearity of the system was examined over the entire intended frequency band of operation. Figure 2.14 represents the obtained output spectrum from the AWR simulation. As shown, the simulated radar system exhibits a strong tone at 70 MHz which corresponds to the range profile of the target. As labeled on the graph, a high in-band dynamic range of 92.73 dB and out-of-band dynamic range of 117.18 dB are achieved in the simulation. The magnitude of the second harmonic at 140 MHz is low compared to the fundamental tone at 70 MHz. This result validates the overall linearity of the miniaturized radar system when excited with wideband input signals. The selected BPFs are suitable for rejecting the IMDs and the undesired frequency bands. Hence, the selected surface mount components are suitable options to replace the discrete microwave components in the small-scale radar testbed. The system is ready to be shifted to PCB-level integration. However, impedance optimization is essential in order to enhance the impedance level of each stage at the desired frequency bands to match the characteristic impedance of the system. This prevents additional losses in the system by reducing the signal reflections at the interconnects of different stages.

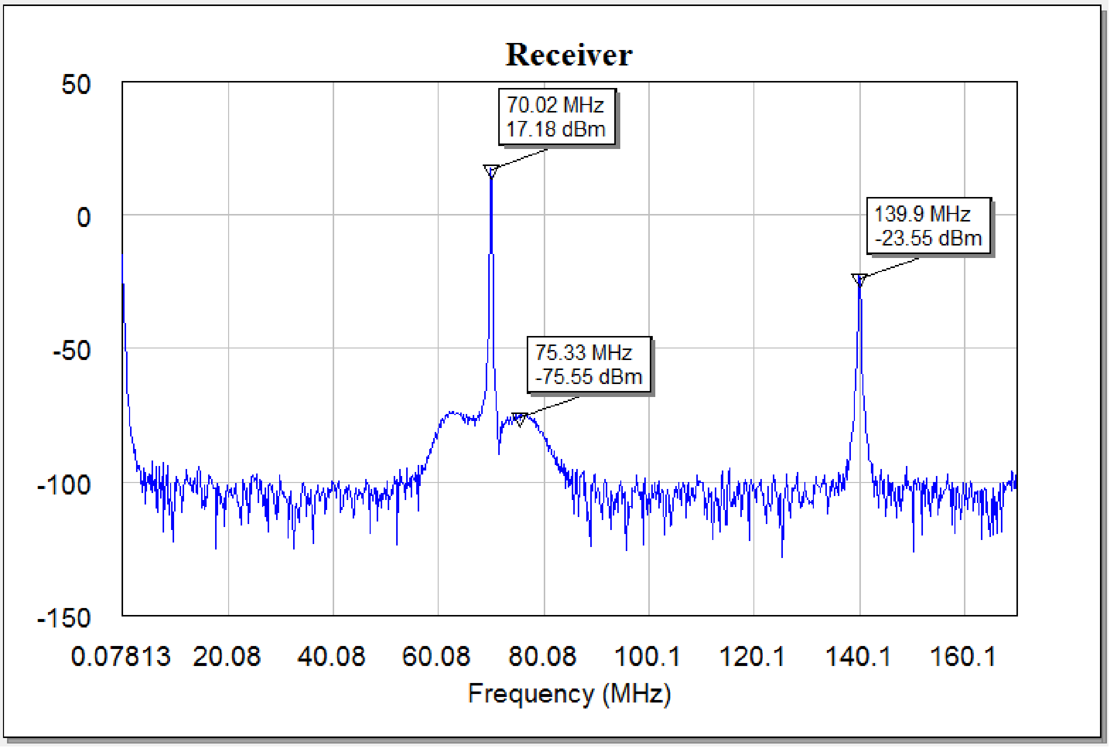


Figure 2.14: Output spectrum of RX channel for baseband LFM chirp (200-500 MHz) input signal.

Chapter 3: Filter Design

In the following chapter, the scattering parameters for two port networks are described first. Then the theory and design of microstrip and coupled microstrip lines required for the design of planar filters are provided. Consequently, the theoretical background and the actual design and simulations of the utilized band pass filters (BPFs) in the radar testbed for PCB are presented.

3.1 Scattering Parameters (S-parameters)

Scattering parameters (S-parameters) are considered as voltage-forward travelling or reflecting waves which are normalized to a known impedance level. In other words, the incoming and outgoing voltage wave incidents at the ports of an *N*-port network are defined by S-parameters which, when squared, are equivalent to the power travelling along the line. These S-parameters are usually defined as a function of frequency for an *N*-port network [25]. The practical S-parameters of such networks in the frequency domain are measured using a vector network analyzer (VNA).

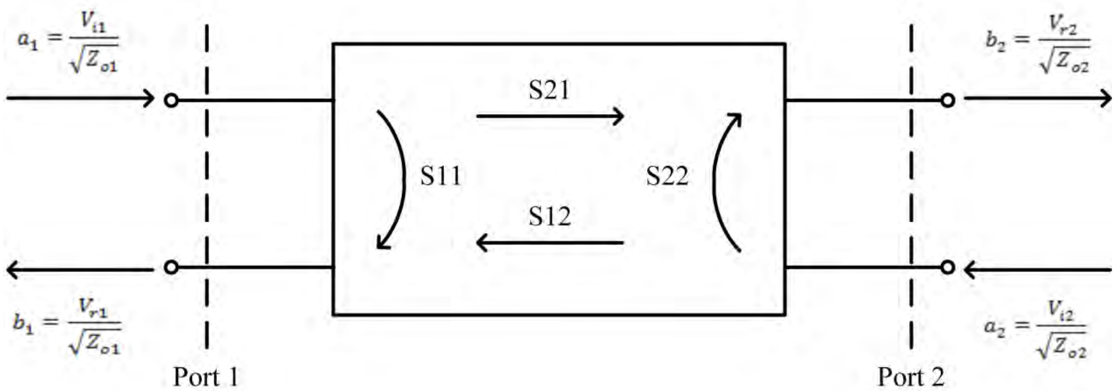


Figure 3.1: Two port network and scattering parameters.

Figure 3.1 above represents a two-port network with a_n considered as the incident waves on port n and b_n considered as the reflected waves from port n along with its S-parameters. The incident waves a_n are considered as the independent variables (port inputs) and the reflected waves b_n are considered as the independent variables (port outputs). These independent variables are defined by [26]:

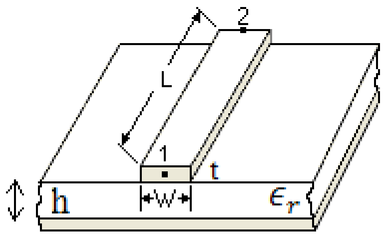
$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{3.1}$$

The reflection coefficient defines how well the impedance of the network is matched to the defined characteristic impedance of the system. It is desired to minimize the reflection as much as possible to reduce power loss in the circuit by proper impedance matching. For reciprocal networks such as filters, the reflection and transmission coefficients at both ports are identical due to the symmetrical structure of the circuits.

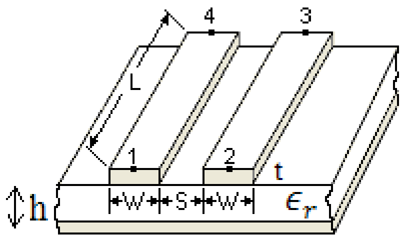
3.2 Single Microstrip and Coupled Microstrip Lines

Microstrip lines are the most popular transmission line structure in microwave integrated circuits (MIC), as they can be easily integrated with other electronic circuitry. Microstrip lines are widely used in microwave devices due to their design simplicity and ease of fabrication by photolithographic processes. The other advantages of microstrip lines are low weight, small size, and having a wide bandwidth. The drawback of these transmission lines is their low power capabilities and high attenuations. A microstrip line consists of a conductor with a width (W), length (L), and thickness (t) which is printed on the top of a ground plane conductor, separated by a dielectric substrate with a defined relative permittivity (ε_r) and thickness (h), as shown in Figure 3.2 (a). In [27], the design equations for different parameters of a single microstrip line are provided.

As shown in Figure 3.2 (b), the microstrip coupled lines are created by placing two single microstrip lines with some spacing (S) next to each other. According to the coupled line theory, EM interaction occurs when two transmission lines are placed closely together in a parallel configuration which results in power coupling between the lines [28, 29]. The return path for the RF currents in microstrip geometries is done through the bottom layer of the PCB which is made of a conductor and acts as a ground plane. The detailed design equations of coupled microstrip lines are presented in [30]. More accurate models and numerical solutions are used in modern CAD tools such as LineCalc to calculate the dimensions and the characteristic impedances of microstrip geometries.



(a)



(b)

Figure 3.2: Geometry of (a) Microstrip line (b) Microstrip coupled line.

The attenuations in the microstrip lines are due to the dielectric and conductor materials of the PCB. The dielectric loss is related to the relative permittivity of the substrate (ε_r), the effective dielectric constant (ε_{eff}), and the loss tangent of the dielectric ($\tan\delta$). The conductor loss, which is mainly due to the surface resistivity of the conductor, is inversely proportional to the width and impedance of the microstrip line. At higher frequencies, the radiation loss should be taken into account, and can be minimized by reducing the number of discontinuities in the design and the proper selection of substrate material. In general, thinner materials with higher dielectric constants result in lower radiation losses in microstrip structures.

3.3 PCB Material

3.3.1 PCB Material Specifications

The selection of the substrate material and thickness of the PCB is important in the design of RF and microwave circuits. The dielectric constant and thickness of the desired material should be specified in advance in order to design the equivalent microstrip lines, coupled microstrip lines, and patches for the desired planar circuits. As discussed in the microstrip lines section, the physical dimensions of these circuits vary when the same circuits are designed on different substrate materials or thicknesses. In addition, the selected PCB material should be rigid enough to handle the entire passive and active components when soldered (assembled) to the board. One of the trade-offs in choosing a material for PCBs operating at high frequencies is between the cost and the performance [31]. The price of the raw material and its required fabrication efforts and processes are the key factors in specifying the overall cost of the final product. The selection of the material should be based on the required needs of certain applications in which the circuits are intended to be used for.

The selection of the laminate is based on the material properties, circuit fabrication issues, and the end-user requirements based on the desired application and environment [32]. The material properties include the electrical performance and parameter tolerances. The electrical performance of the substrate material is mainly determined by the relative permittivity (or dielectric constant ε_r), thickness (h), and the dissipation factor (or loss tangent $\tan\delta$). The lower tolerance of determining parameters such as the dielectric constant is of interest for applications where higher controlled impedance is required to achieve the designated impedances after fabrication. The dissipation factor is an indication of the dielectric loss in the specified material. A lower value of this parameter indicates a lower dielectric loss in the substrate and vice versa. Other types of losses in such circuits are the conductor and radiation losses. The conductor losses in the circuits are associated with the quality, type, surface roughness, thickness of the utilized conductor, circuit configuration, and substrate thickness. The radiation losses in the microstrip lines are dependent upon the frequency of operation and the laminate thickness [33].

Other parameters in the selection of the substrate material are the thermal coefficient of ε_r, thermal conductivity, surface, and volume resistivity. The effect of thermal behaviour of the material is important at the fabrication time as well as the final PCB assembly. Circuit fabrication (process) issues include the thermal behaviour as well as the etching, drilling and plating conditions of the material.

3.3.2 PCB Material Selection for thesis

For this research, a Rogers RT/Duroid 6010 microwave laminate with a dielectric constant (ε_r) of 10.2, loss tangent ($\tan\delta$) of 0.0023, 50 mils (1.27 mm) thickness, 1 oz (35 μm) finished copper cladding (copper weight), and 0.01%

moisture absorption is selected [34]. The reason for selecting a high permittivity material is to achieve the required circuit performances by having more compact circuits on the PCB. Unlike other high dielectric constant materials, RT/Duroid 6010 laminate is a high dielectric constant ceramic/PTFE composite designed for microwave circuit applications with very low moisture absorption which results in more stable responses in humid environments [35]. The low dissipation factor (loss tangent) of this laminate at high frequencies is favourable which reduces the dielectric losses in the circuits. As mentioned before, the radiation losses are decreased by utilizing thinner laminates. However, the fabrication of thinner laminates is difficult due to their handling and dimensional stability [33]. In addition, a thin laminate is not capable of handling a considerable amount of lumped components and RF connectors to be assembled on. Hence, the standard 50 mils thickness is a proper selection to ease the assembly and fabrication for this research study.

Figure 3.3 shows the substrate model used for the computer simulation (Momentum ADS) of the designed circuits in this thesis. As shown, the board consists of two conductor layers which are specified to be copper with 35 μm thickness. The upper conductor layer is used to create different circuits such as planar filters and to assemble the required ICs. The bottom conductor layer is used as a ground plane to build a microstrip planar structure. The substrate material is defined to be a Rogers RT/Duroid 6010 laminate from the material database of ADS (the parameters are the same as the Rogers 6010 laminate datasheet). The copper connection through the substrate defines the locations of via holes which are used to connect the upper conductor layer to the bottom one for grounding purposes.

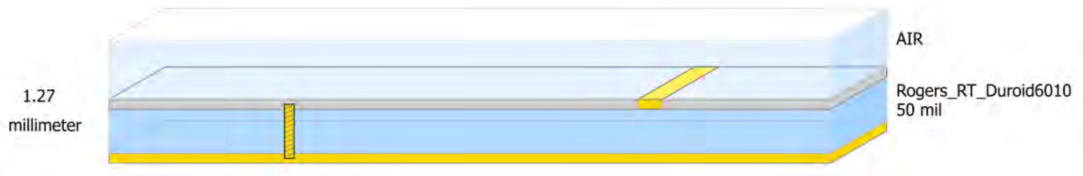


Figure 3.3: Substrate model in ADS.

As it is seen, the Rogers laminates consist of two copper layers and an insulation layer in between. These laminates do not have any photoresist layers on the top of the conductor layers. The fabrication of Rogers laminates was not possible with the available on-campus facilities. Hence, FR4 substrate with a dielectric constant (ε_r)

of 4.55, loss tangent ($\tan\delta$) of 0.0175, 63 mils (1.6 mm) thickness, 1 oz (35 μm) finished copper cladding (copper weight), and 0.12% moisture absorption was utilized for initial tests and on-campus fabrications. Table 3.1 below summarizes different specifications of the utilized PCBs in this research.

Table 3.1: Properties of the used substrates in this research.

Property	Symbol	RT/Duroid 6010	FR4	Unit
Dielectric Constant	ε_r	10.2	4.55	-
Loss Tangent	$\tan\delta$	0.0023	0.0175	-
Substrate Thickness	h	1.27	1.6	mm
Copper Weight	t	35	35	μm
Moisture Absorption	-	0.01	0.12	%

Compared to the RT/Duroid 6010 laminate, the normal FR4 has a lower dielectric constant which increases the overall size of the circuits. In addition, it has a very high loss tangent which increases the dielectric losses in the board itself. The moisture absorption of the Rogers laminate is much better as well. Hence, RT/Duroid 6010 is a better laminate for the radar testbed as an intended application of this research.

3.4 Importance of Filters for Radar Testbed

Filters are one of the most important components in communication systems as they are aimed to reduce the overall spurious products in the system [36]. Filters are characterized by insertion loss and selectivity which are related to the specifications of the pass band and attenuation bands, respectively. An ideal filter is a filter with no insertion loss and infinite attenuation at the out-of-band frequencies. However, such an ideal filter is not achievable in practical scenarios. Generally, a filter with a lower insertion loss and a higher (acceptable) selectivity (or out-of-band attenuation) is of interest [37].

Several filters are required for the proposed digital radar system as was shown in the system level architecture. Filtering is an important task in both the transmitter and the receiver channels. In both channels, nonlinear devices such as mixers and frequency doublers are utilized to perform the frequency transformation in which IMDs are produced. Strong IMDs could drive the system into saturation, which reduces the dynamic range. Four different BPFs operating at different frequencies are required for the TX and LO channels in addition to the two required filters for the RX channel. The proposed digital array radar system has only one TX and LO channel and several replicas of receiver channels. Hence, designing the desired BPFs will reduce the cost of the overall system as well.

3.5 Summary of the Utilized BPF Types for the Radar Testbed

The size of the filter is a function of the wavelength, which is inversely proportional to the operation frequency. In other words, the size of the filters decreases at higher frequencies compared to lower frequencies due to the decrease in the operational wavelength. At higher frequencies such as microwave ranges, lumped inductor and capacitor components cannot be utilized due to the reduced quality factors [38, 39]. Thus, distributed elements are an appropriate choice for the filter implementation at such high frequencies. While planar microstrip filters are suitable options for filters operating at higher frequencies (>1 GHz), the size of such filters increases dramatically at lower frequencies (<1 GHz). Hence, in this research, microstrip planar BPFs are designed for the TX and LO channels due to their operation frequencies which are greater than 1 GHz. On the other hand, a hybrid filter design of microstrip stepped-impedance resonators (SIR) and lumped components along with a filter with lumped components are chosen for the RX filters.

Chebyshev filters are chosen for the design of the filters in this thesis. The reason for this selection is the better attenuation characteristics of the Chebyshev filters in the stop band compared to the Butterworth filters of the same order (number of filter stages). The better out-of-band rejection characteristics of Chebyshev filters is due to the added ripples in the pass band at the expense of causing additional group delay in the signal path [40]. Bessel filters provide maximally flat group delays which result in a linear phase response of the filter. This linear phase response is of interest in avoiding distortion in the wideband signals. Hence, the selection of filter category is a compromise of different parameters and depends on the application's requirements.

For the design of BPFs, the insertion loss method which utilizes a network synthesis technique to meet the specifications of the desired filter over the whole frequency bands is used [41]. In all filters initially, the element values of the normalized LPF prototype are extracted from the available tables [42]. Then these elements are transformed into the equivalent components to design the required BPFs.

The BPF is a filter which passes the desired band of frequencies $(\omega_1 - \omega_2)$ which is defined as the filter's bandwidth. The center frequency of the filter is defined as [43]:

$$\omega_o = \sqrt{\omega_1 \, \omega_2} \tag{3.2}$$

and the fractional bandwidth is defined as the ratio of the filter bandwidth and the center frequency as given in equation (3.3) below.

$$\Delta = \frac{\omega_2 - \omega_1}{\omega_o} \tag{3.3}$$

3.6 Parallel Coupled Line BPF

Parallel coupled line (CL) band pass filters are widely used in microwave and communication systems. Coupled line filters are created by cascading groups of coupled microstrip line sections of the same electrical lengths. The length of each coupled section is a function of the wavelength $(\theta = {}^{\pi}/_{2})$, introducing quarter-wavelength coupled lines at the center frequency of the filter [44]. These types of filters are suitable for high frequency applications with up to 20% of fractional bandwidths. Wider fractional bandwidths are not achievable due to the tight required coupling between the coupled lines which cannot be practically fabricated [45]. Microstrip BPFs with wider bandwidths are achievable by utilizing other filter structures such as connecting short circuit stub lines and parallel stubs of ${}^{\lambda}/_{4}$ lengths [46].

According to the microwave theory, these quarter-wavelength CLs are equivalent to parallel inductor and capacitor resonator circuits and the spacing between them corresponds to the admittance inverters (J-inverters) [47]. The detailed design equations of the parallel CL filters are given in [27].

The design of the parallel CL BPF is simple and uses a straightforward procedure. Other advantages of this structure lie in its simple planar structure, low cost, low weight, and easy integration with other electronic circuitry. The fabrication of this filter structure is highly practical as the structure does not require any ground connections (by utilizing via holes) and is easily fabricated [48].

3.6.1 Coupled Line BPF on FR4 Substrate

In order to realize whether the overall radar system could be developed and fabricated on-campus, it was proposed to design, fabricate, and test some RF circuits using the available FR4 substrates. The parallel CL filter was chosen for this task due to its simple design and fabrication.

3.6.1.1 Design of narrow bandwidth filter

A BPF with a center frequency of 1.67 GHz and 10% fractional bandwidth (Δ) was targeted to be designed and fabricated. As for the first trial, the design bandwidth was reduced to 167 MHz rather than the required filter with 300 MHz bandwidth for the radar system. The reason for this decision was to avoid the problems of having wideband design with the available on-campus substrate which is not desired to operate at high frequencies. A third-order Chebyshev filter with a 0.5 dB ripple was selected and the elements of the normalized LPF prototype were extracted using the available tables. A 3-stage CL BPF consists of four sections of parallel lines. Consequently, the even- and odd-mode characteristic impedances were calculated using a developed MATLAB code. Table 3.2 represents different stages of the filter along with the extracted elements of the normalized LPF prototype and the calculated even- and odd-mode characteristic impedances.

As seen in Table 3.2, the parameters of the first and the last stages along with those of the second and third stages (intermediate stages) are the same to produce a symmetrical structure. Figure 3.4 shows the ADS circuit simulation (S-parameters) of the designed BPF using ideal components (Z_{oe} and Z_{oo}) with the specified center frequency and the electrical lengths.

The calculated impedances in Table 3.2 were inserted in the LineCalc tool with the specifications of the FR4 substrate to extract the dimensions (W, S, and L) of different parallel coupled stages. Figure 3.5 presents a screenshot of the LineCalc tool for the first stage calculations. As seen in Figure 3.5, the design center frequency is entered to be 1.67 GHz and the electrical length of the lines is specified to be 90° to generate quarter-wavelength coupled lines. Table 3.3 shows the extracted dimensions of the parallel CL for each stage of the filter.

Table 3.2: Calculated even- and odd-mode characteristic impedances of CL BPF (f_o = 1.67 MHz, Δ= 0.1).

n	$g(n)$	$Z_{oe}(\Omega)$	$Z_{oo}(\Omega)$
1	1.5963	70.605	39.235
2	1.0967	56.639	44.769
3	1.5963	56.639	44.769
4	1	70.605	39.235

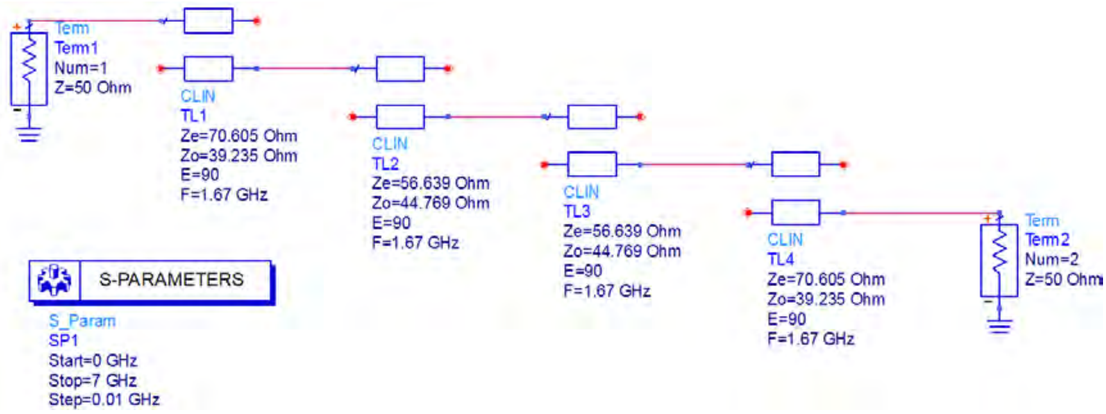


Figure 3.4: Schematic simulation of CL BPF in ADS (ideal components).

Figure 3.6 shows the circuit simulation of the designed BPF using microstrip CLs in ADS. As shown in the figure, the "MSub" component defines the FR4 substrate with the specified parameters. Two 50 Ω microstrip lines with a width of 2.952 mm and length of 5 mm are added to both terminals of the filter to enable the soldering of the SMA connectors to the PCB. In addition, microstrip lines of 0.381 mm lengths are added between stages (1, 2) and (3, 4) to avoid shorting the CLs of different stages in the layout.

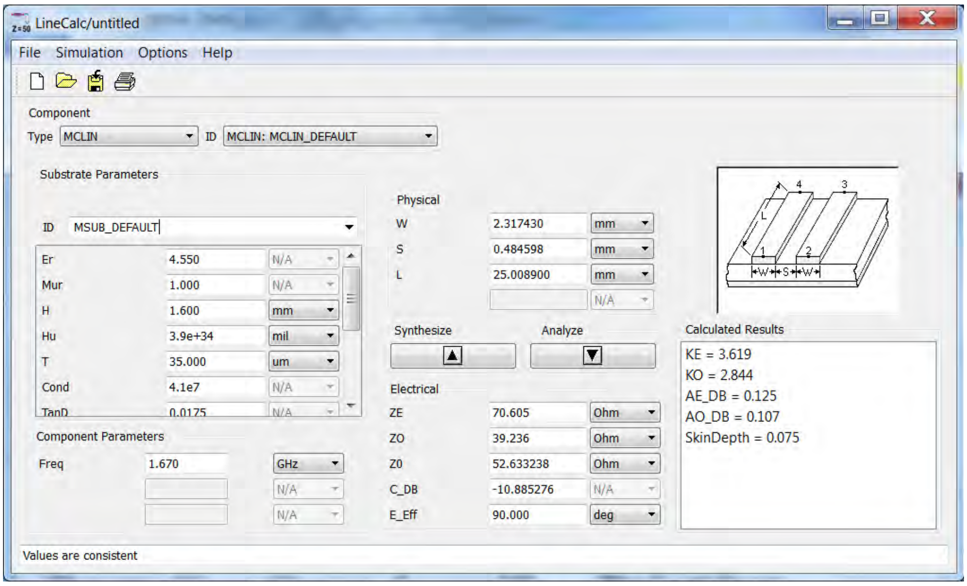


Figure 3.5: LineCalc tool.

Table 3.3: Calculated dimensions of CL BPF ($f_o = 1.67\ MHz, \Delta = 0.1$) for FR4 substrate.

n	$W(mm)$	$S(mm)$	$L(mm)$
1	2.317	0.485	25.009
2	2.836	1.793	24.450
3	2.836	1.793	24.450
4	2.317	0.485	25.009

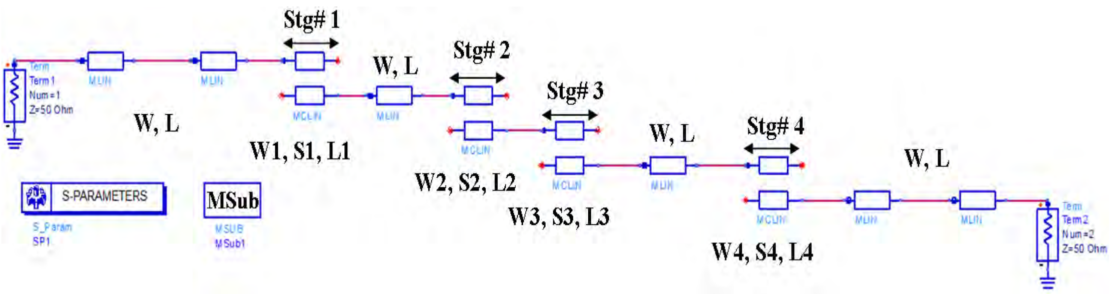


Figure 3.6: Schematic simulation of parallel CL BPF in ADS (microstrip components).

The discussed circuit simulations (ideal and microstrip simulation) are not precise enough to simulate the structure of such BPFs. Hence, the filter structure should be simulated using EM simulators such as the Momentum simulator of ADS to produce the actual response of the filter. Figure 3.7 shows the constructed layout of the designed parallel CL BPF with the created mesh during simulation. The mesh frequency in the simulation setup was set to 10 GHz and the mesh density was specified to be 30 cells per wavelength. This is a good and high resolution setup for the desired frequency range of simulation.

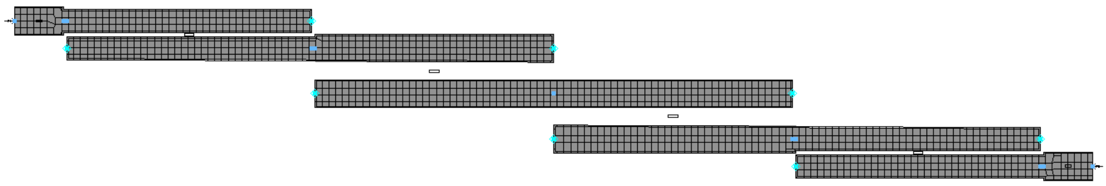
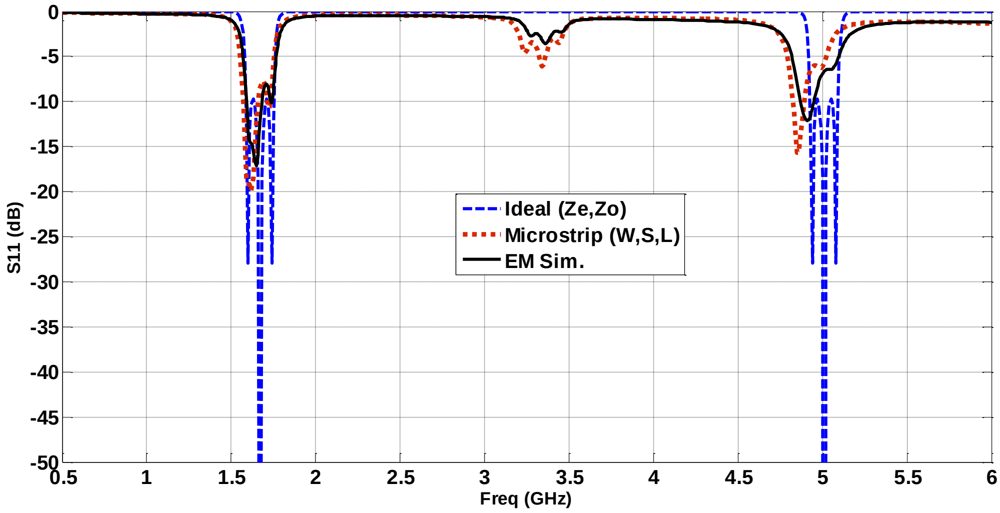


Figure 3.7: Layout simulation of parallel CL BPF in ADS (Momentum).

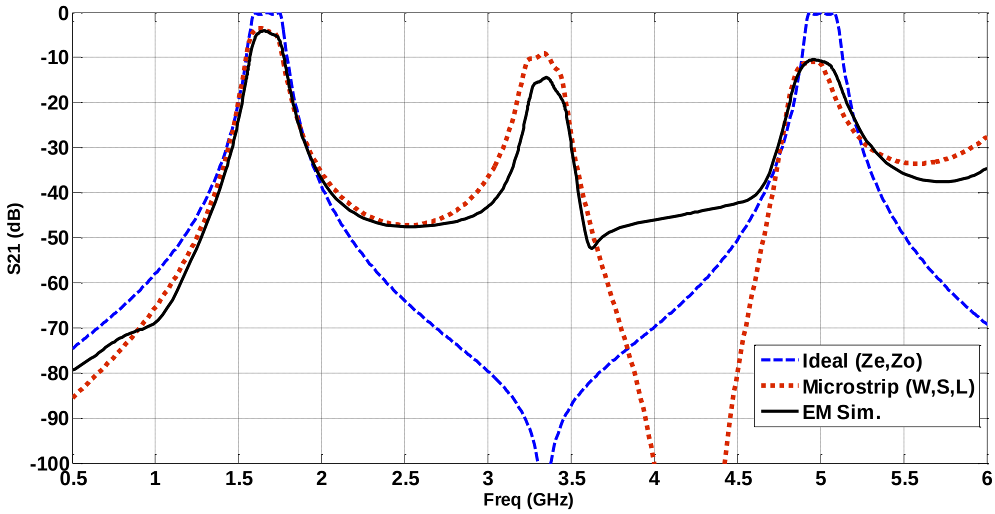
In Figure 3.8, a comparison between the S11 and S21 results of the ideal circuit, microstrip circuit, and layout simulation is provided. The S11 response represents the return loss and the insertion loss is extracted from the S21 response of the filter. As shown in the figures, the ideal circuit simulation exhibits a perfect BPF response at the designated frequency band with a 1.67 GHz center frequency. The fundamental BPF response is repeated in a periodic pattern over the frequency. The first spurious response of the ideal simulation occurs at the third harmonic of the fundamental frequency. Hence, this simulation is not good enough for practical applications. The microstrip simulation produces more accurate results which are closer to the result of layout simulation. The difference between these two simulations is in the required simulation time. The circuit simulation is much faster than the layout simulation and is fair enough for the initial idea about the response of the structure and dimensions optimization. However, this simulation is not recommended for non-standard structures as the exact coupling could not be simulated accurately.

The S21 phase responses of these simulations are shown in Figure 3.9. As it is seen, all types of simulations confirm a linear S21 phase response for the designed parallel CL filter over the desired pass band of the filter.

The designed parallel CL BPF was fabricated on-campus using the specified FR4 substrate. Figure 3.10 shows the fabricated BPF with the soldered 50 Ω SMA connectors to enable the measurements of the BPF response using VNA. Before the measurements, the VNA was calibrated using the calibration kit with standard short circuit, open circuit, and matched loads.



(a)



(b)

Figure 3.8: Comparison between responses of initially designed parallel CL BPF in different simulations (a) S11 magnitude (b) S21 magnitude.

The S11 and S21 comparison between the EM simulation and the measurements of the filter are shown in Figure 3.11. In comparison, the measured return loss matches the simulated return loss over the desired bandwidth. However, a 50 MHz shift in the center frequency towards the higher frequencies is observed between the simulation and the measurements. This frequency shift in the response of the filter is noticeable from the S21 comparison plot.

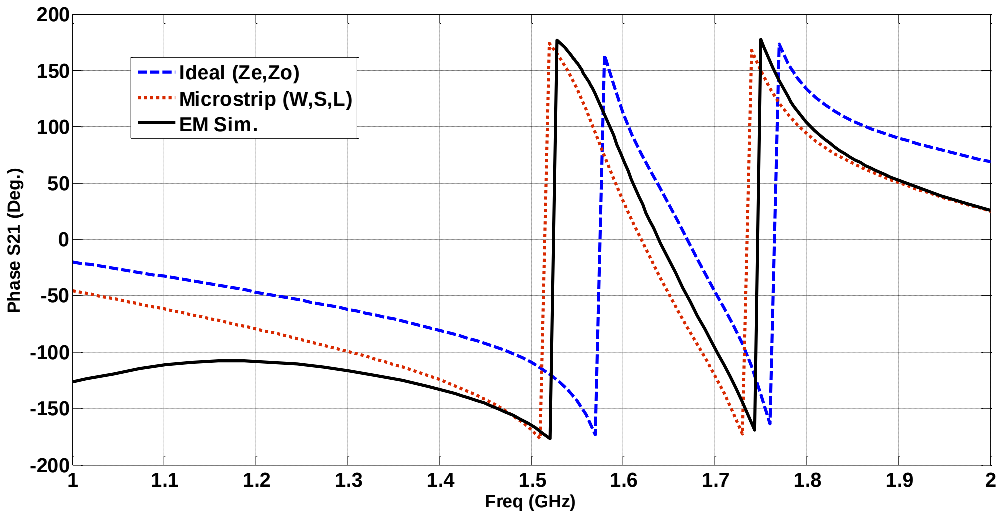


Figure 3.9: Comparison between S21 phase responses of initially designed parallel CL BPF in different simulations.

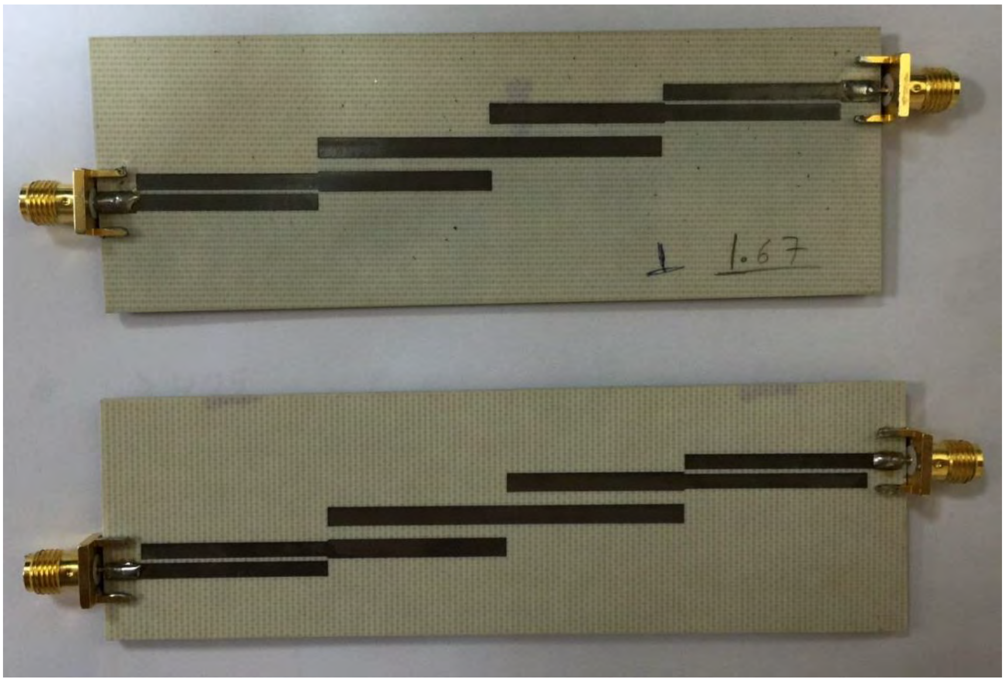
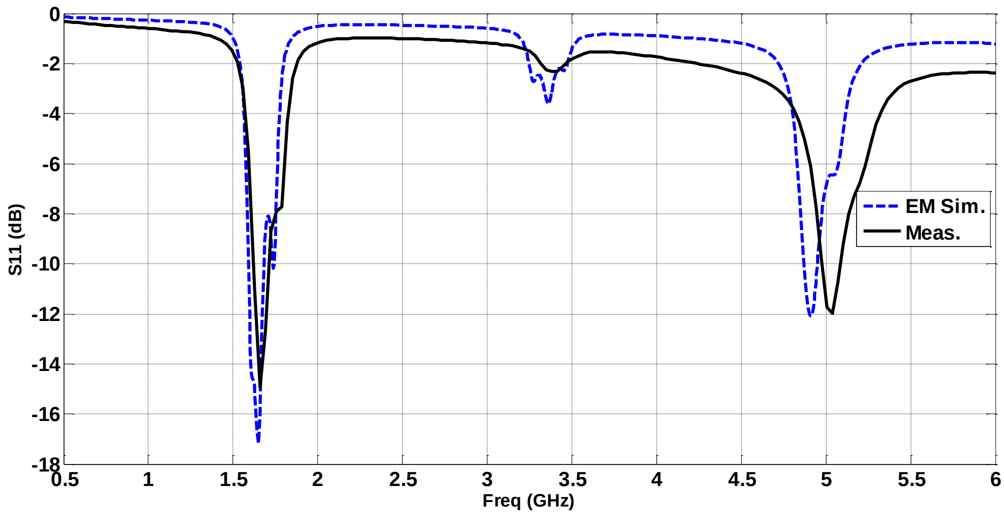
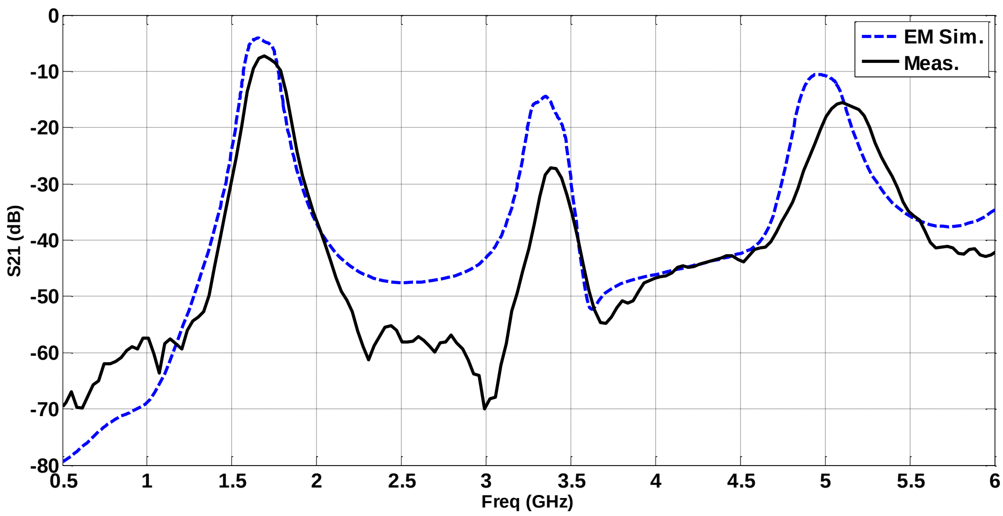


Figure 3.10: On-campus fabricated parallel CL BPFs with different center frequencies.

The changes in the fabricated dimensions of the coupled lines due to the fabrication tolerances as well as the actual properties of the utilized board (exact value of the dielectric constant at operating frequency) can be considered the main reasons for the mentioned frequency shift. In addition, the insertion loss of the filter is further increased indicating higher loss in the filter by using the lossy FR4 substrate. This is not desired for the radar testbed. In contrast to this frequency shift, the measured bandwidth of the filter is very close to the simulated one. Hence, this frequency shift should be considered at the design stage of the filter to reach the desired center frequency after fabrication.



(a)



(b)

Figure 3.11: Simulated vs. measurements of initially designed parallel CL BPF (a) S11 magnitude (b) S21 magnitude.

The same CL filter was redesigned to consider the measured shift in the center frequency (Figure 3.10). The comparison between the EM simulation and measurement of the new parallel CL BPF with a design center frequency of 1.57 GHz is shown in Figure 3.12. In addition, the measurement results of the previous filter are plotted to verify the shift in the center frequency of the new fabricated filter.

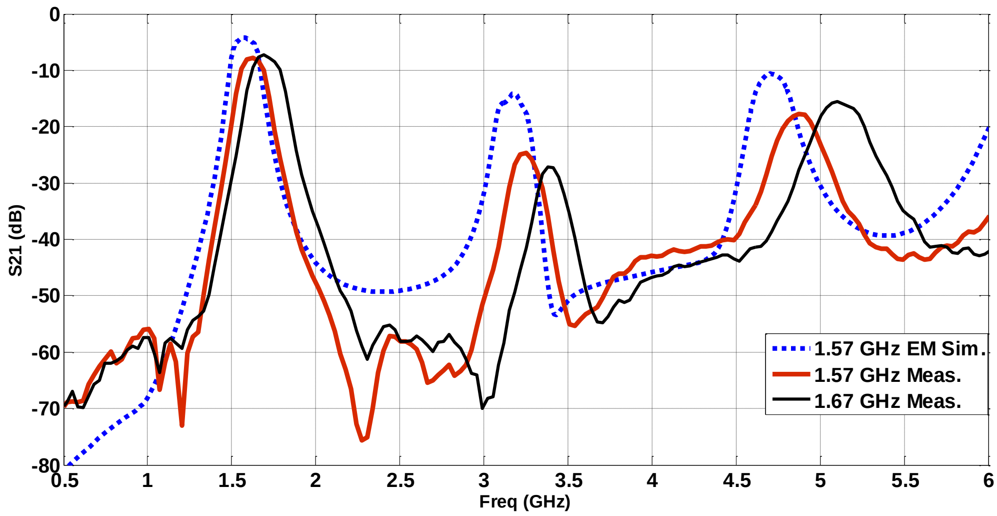


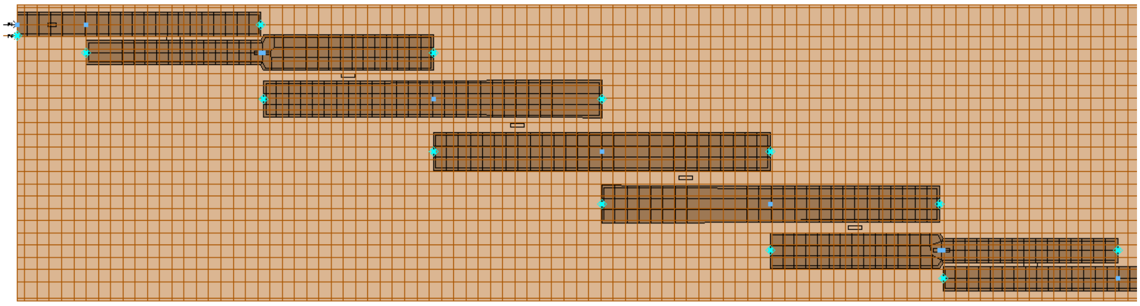
Figure 3.12: Simulated vs. measured comparison of S21 for the two fabricated parallel CL BPFs.

3.6.1.2 Design of wider bandwidth filter

In the previous implementations, filters with 10% fractional bandwidths were designed. However, in the TX and LO channels of the radar testbed, filters of much wider bandwidths are required. Hence, the on-campus fabrication was examined by the design and implementation of a new BPF with higher center frequency and wider bandwidth. In order to have better out-of-band rejection levels with reduced ripples in the pass band, a fifth-order Chebyshev filter with a 0.2 dB ripple was selected. The second filter of the TX channel with a center frequency of 3.34 GHz and 20% fractional bandwidth was chosen for this design. Table 3.4 represents the specifications of the designed BPF.

Table 3.4: Specifications of designed parallel CL BPF on FR4 substrate ($f_o =$ 3.34 $GHz, \Delta =$ 0.2).

n	$g(n)$	$Z_{oe}(\Omega)$	$Z_{oo}(\Omega)$	$W(mm)$	$S(mm)$	$L(mm)$
1	1.3394	85.943	37.512	1.788	0.255	12.731
2	1.337	64.494	41.018	2.593	0.786	12.344
3	2.166	60.935	42.474	2.728	1.104	12.267
4	1.337	60.935	42.474	2.728	1.104	12.267
5	1.3394	64.494	41.018	2.593	0.786	12.344
6	1	85.943	37.512	1.788	0.255	12.731



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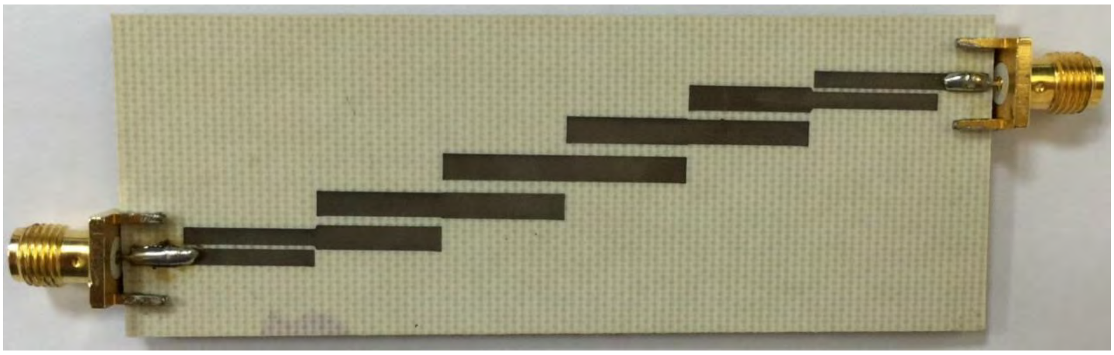


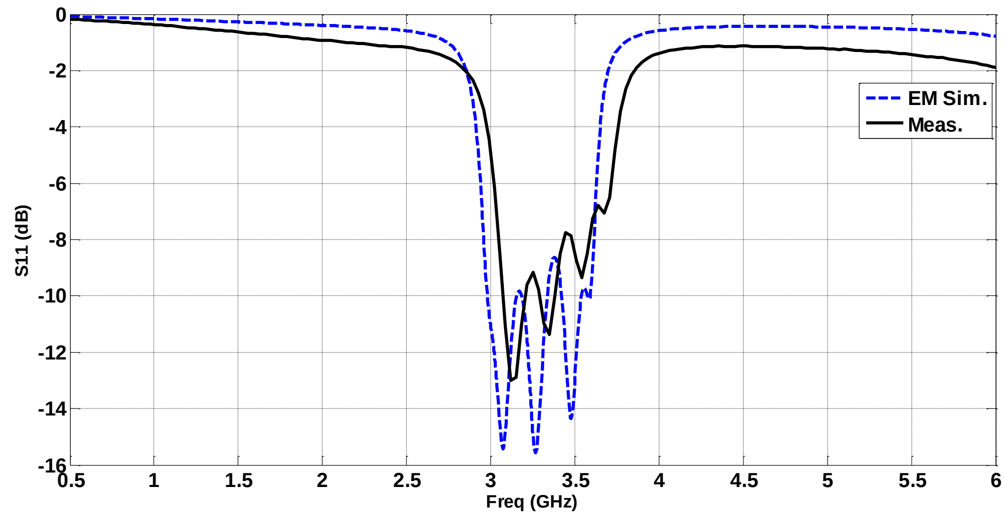
(b)

Figure 3.13: Designed parallel CL BPF with $f_o = 3.34\ GHz$ on FR4 (a) Layout simulation (b) Fabricated.

Figure 3.13 depicts the simulated layout and fabricated CL BPF on the FR4 substrate with a center frequency of 3.34 GHz. The response of the filter was measured using VNA and the comparison between the simulated and measurement results are plotted in Figure 3.14. Based on the measured return loss response, the majority of the signal is reflected back from the pass band of the filter which causes additional power loss in the filter. This is due to improper impedance matching between the filter and the measurement's characteristic impedance (50 Ω) at the operation frequencies. In addition, the measured S21 indicates further reduction in the bandwidth of the filter which is not convenient.

From the presented results of the on-campus fabricated filters, it is concluded that the available FR4 boards and available fabrication facilities are not suitable for high frequency applications with wide operating bandwidths. The implementation of the radar system using the available FR4 boards results in lossy RF circuits which increase the complexity of the overall system in order to achieve the required goals.

As inferred from the difference between the simulation and measurement results, the computer simulations at high frequencies are not guaranteed for this low quality fabrication. Hence, high frequency laminates with high standard fabrications (with low tolerances) are desirable for the PCB implementation of the overall radar system.



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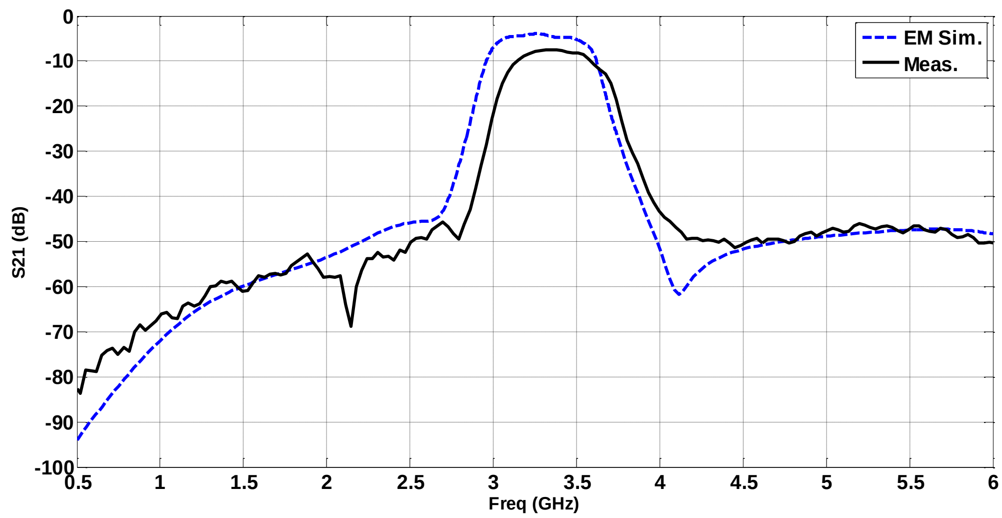


(b)

Figure 3.14: Simulated vs. measurements of 3.34 GHz parallel CL BPF (a) S11 magnitude (b) S21 magnitude.

3.6.2 Coupled line BPF on Rogers RT/Duroid 6010

In order to use the high quality Rogers substrate, the frequency shift between the schematic and the layout for this substrate should be known. Hence, a fifth-order, 0.2 dB ripple Chebyshev CL BPF with a center frequency of 3.4 GHz and 24.7%

fractional bandwidth (2.98-3.82 GHz) was designed and simulated. In the EM simulation, the lower limit of the bandwidth was significantly unaffected and the upper limit was reduced, indicating a reduction in the overall bandwidth of the filter and a shift in the center frequency. This reduction in the bandwidth and a higher center frequency should be considered at the design stage of the filter to meet the desired specs. Hence, the same filter was redesigned for 3.01-3.95 GHz with a center frequency of 3.45 GHz. The fractional bandwidth of the filter is 27.2%, which is more than the desired value to remain in the margins for the fabrication tolerances. Table 3.5 summarizes the specifications of different CL stages of this filter.

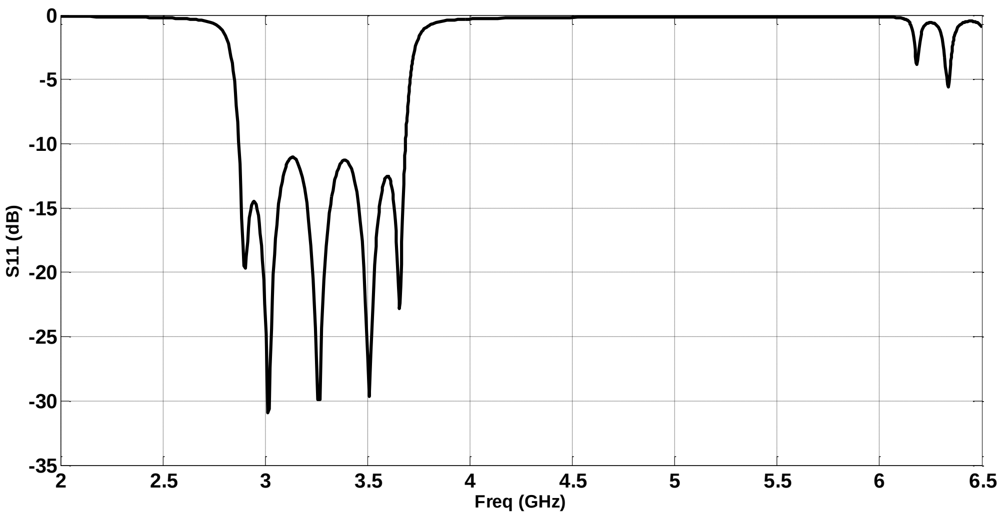
Table 3.5: Specifications of re-designed parallel CL BPF ($f_o = 3.45\ GHz$).

n	$g(n)$	$Z_{oe}(\Omega)$	$Z_{oo}(\Omega)$	$W(mm)$	$S(mm)$	$L(mm)$
1	1.3394	94.189	37.710	0.513	0.286	8.872
2	1.337	71.061	39.133	0.862	0.555	8.549
3	2.166	65.705	40.598	0.954	0.749	8.466
4	1.337	65.705	40.598	0.954	0.749	8.466
5	1.3394	71.061	39.133	0.862	0.555	8.549
6	1	94.189	37.710	0.513	0.286	8.872

The overall size of the layout of the filter is $56.8 \times 10.8\ \mathrm{mm}^2$. Figure 3.15 presents the EM simulation results of this filter. As seen from the plots, the bandwidth of the filter in the EM simulation is 2.9-3.65 GHz which includes the desired pass band frequencies for the second filter of the radar's TX channel (3.04-3.64 GHz). Within this pass band, the return loss is well below -10 dB, indicating a good impedance matching between the filter and 50 Ω characteristic impedance of the system. In addition, the insertion loss of the filter is much less compared to the FR4 substrate due to the better quality of the Rogers substrate with less loss tangent. However, the magnitude of the spurious response is increased due to the increase in the dielectric constant of the substrate.

The phase of S21 is linear over the entire pass band of the filter. This indicates a linear phase shift in the signals at all frequencies within the filter's pass band. The propagation delay of a signal within any circuit is defined as the slope of the phase response of that circuit. Hence, the linear phase shift in the filter results in a constant delay for the wideband signals which avoids dispersion of such signals. Dispersion occurs when the circuit has different time delays for different frequency components of a wideband signal. Thus, for having a constant phase delay with respect to frequency, a linear phase response over the desired frequencies is necessary.

The parallel CL BPF requires a larger area compared to other microwave filters due to their cascaded CL structure. Hence, miniaturization techniques such as those discussed in [49, 50] could be an appropriate solution for the reduction in the size of these filters. Another solution to have a more compact filter structure is to transform the same design into a hairpin configuration which is discussed in the next section.



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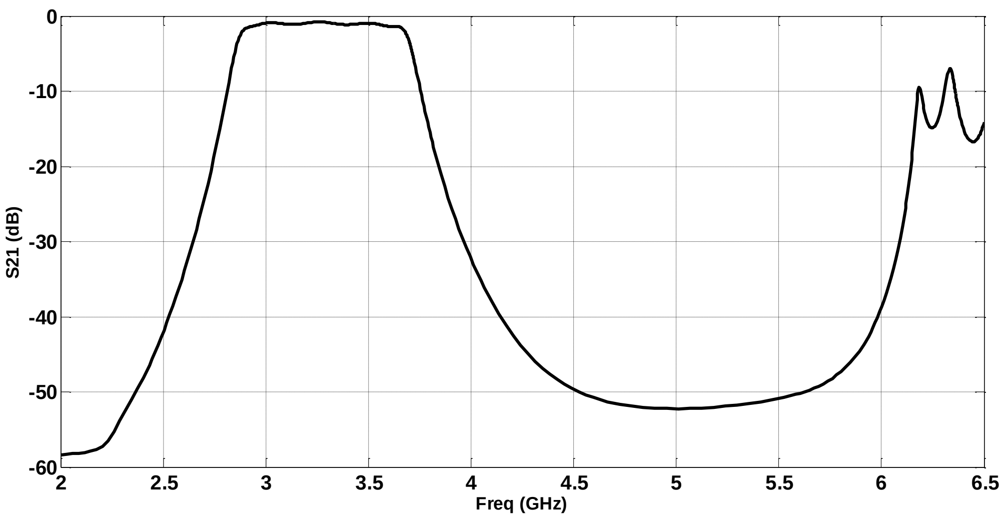

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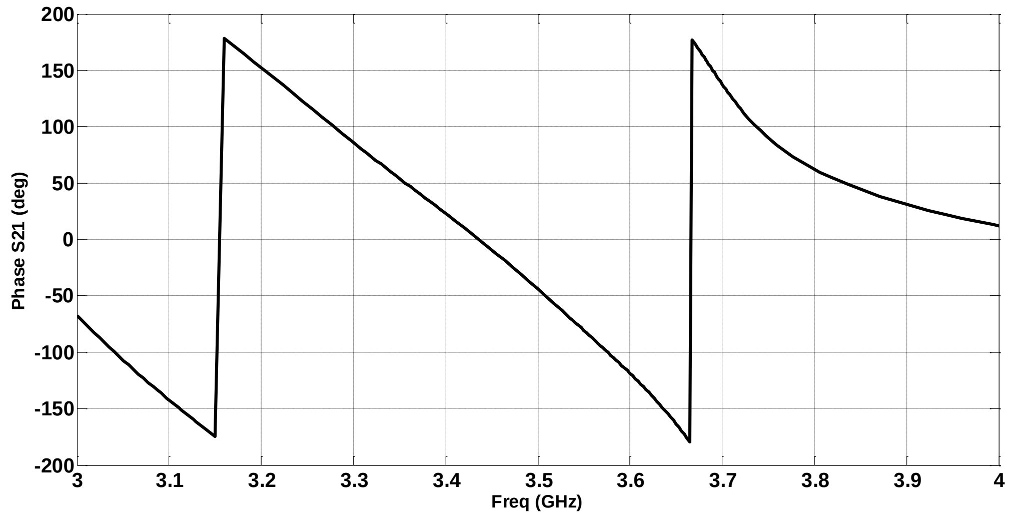


(c)

Figure 3.15: EM simulation of 3.34 GHz parallel CL BPF on Rogers 6010 substrate (a) S11 magnitude (b) 21 magnitude (c) S21 phase.

3.7 Hairpin BPF

Size miniaturization is necessary in order to produce more compact filters which are of interest in today's growing communication systems. The reduction in the size of these systems leads to a reduction in the overall cost of the system as well. Hairpin filters are considered to be the compact version of parallel CL filters. Hairpin structures are created by folding the parallel CL half-wave resonators into a U-shape to reduce the overall size of the filter [51]. Similar to the CL structure, the layout of the hairpin structure is easily fabricated as it has open-circuited ends which do not require any grounding vias. Vias increase the fabrication cost, complexity, and require careful modeling to achieve the desired filter response. However, the hairpin structure is limited by the minimum allowable space between the lines which is due to fabrication constraints [52].

3.7.1 Hairpin Filter (3.04-3.64 GHz)

The design of a hairpin filter from a previously designed parallel CL filter for a 3.04-3.64 GHz range is discussed in the following section. Table 3.6 presents the specifications of a fifth-order Chebyshev CL BPF with a 0.2 dB ripple designed on a Rogers 6010 substrate. The center frequency of the filter is 3.34 GHz with 20% fractional bandwidth.

Table 3.6: Specifications of fifth-order, 0.2 dB ripple Chebyshev parallel CL BPF (f_o = 3.34 GHz,Δ = 0.2) on Rogers 6010 substrate.

n	$g(n)$	$Z_{oe}(\Omega)$	$Z_{oo}(\Omega)$	$W(mm)$	$S(mm)$	$L(mm)$
1	1.3394	85.943	37.512	0.623	0.331	9.057
2	1.337	64.494	41.018	0.974	0.809	8.731
3	2.166	60.935	42.474	1.031	1.058	8.674
4	1.337	60.935	42.474	1.031	1.058	8.674
5	1.3394	64.494	41.018	0.974	0.809	8.731
6	1	85.943	37.512	0.623	0.331	9.057

The design of the hairpin filter is similar to the CL filter to some extent. The concern in designing such filters is to find the appropriate coupling coefficients between the coupled stages as a result of the added distance between them (b_n) and the equalization of all resonators' lengths. The sliding factor is added to allow the proper bending of the lines and to avoid self-coupling between the arms of the resonators [53]. For this purpose, proper optimization should be applied on the designed quarter-wavelength coupled stages to achieve the required filter response using the new hairpin structure. Hence, the optimization cockpit in the ADS simulator was utilized for this purpose. In order to reduce the design time, this optimization was done using the schematic simulator of ADS (Figure 3.16) and accordingly, the EM simulation was performed. Hence, the size of the frequency shift between the schematic and the EM (using the Momentum simulator) responses was obtained and considered in the optimization.

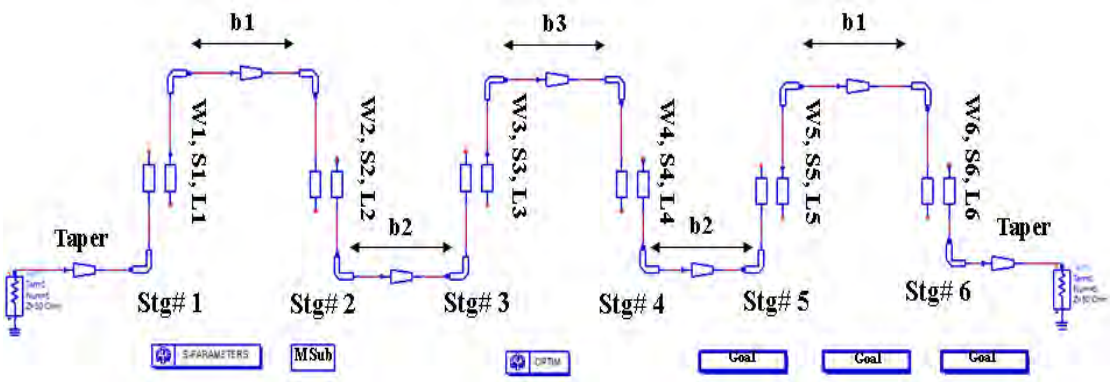


Figure 3.16: Circuit schematic of fifth-order hairpin filter with defined optimization goals.

In the optimization, first the dimensions b_n were optimized for the reduced lengths (L_n) of the resonators. Due to this reduction in the length, the required couplings were achieved by reducing the spacing between the coupled resonators (S_n). Finally, the widths (W_n) of the coupled lines were modified to get the desired filter response.

By comparing the results of the schematic and the EM simulations, it was observed that the lower frequency edge of the pass band was shifted to a higher frequency while the upper frequency edge was not greatly affected. In other words, the overall bandwidth of the filter was reduced; this reduction was considered in the optimization goals, accordingly. The final bandwidth of the filter in the optimization goals was set to 2.78-3.68 GHz and the attenuation frequencies were defined appropriately. Table 3.7 summarizes the final dimensions of different resonator stages of the optimized hairpin filter with a 3.34 GHz center frequency. Figure 3.17 shows the simulated layout of the optimized hairpin filter (with generated simulation meshes) connected to the end-point taper feed lines ($W = 1.156$ mm).

Table 3.7: Specifications of the optimized hairpin BPF ($f_o = 3.34$ GHz, $\Delta = 0.192$) on Rogers 6010 substrate.

$\boldsymbol{n}$	$\boldsymbol{W_n(mm)}$	$\boldsymbol{S_n(mm)}$	$\boldsymbol{L_n(mm)}$	$\boldsymbol{b_{n,n+1}(mm)}$
1	0.587	0.187	7.630	0.386
2	0.728	0.473	7.630	0.132
3	0.741	0.611	7.630	0.131
4	0.741	0.611	7.630	0.132
5	0.728	0.473	7.630	0.386
6	0.587	0.187	7.630	NA

Figure 3.18 presents the EM simulation responses of the optimized hairpin filter. As expected from previous designs, the bandwidth is reduced in the EM simulation as the lower edge frequency of the filter is shifted to a higher frequency point. The bandwidth of the filter in the EM simulation is 3.02-3.66 GHz which is same as the pass band of the desired BPF. The S11 response is almost below -10 dB, indicating proper impedance matching over the entire pass band of the filter. As desired, the phase of S21 is linear over the filter's bandwidth.

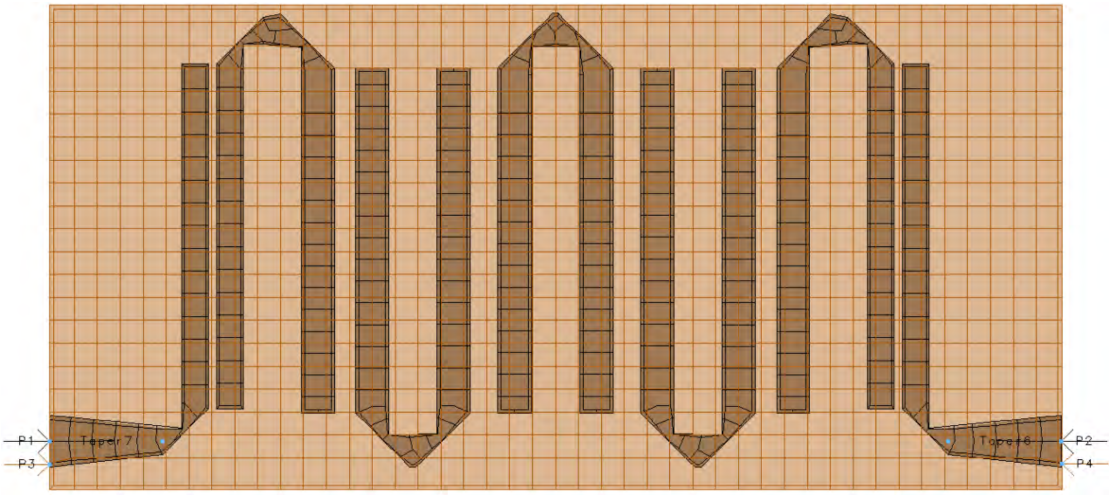
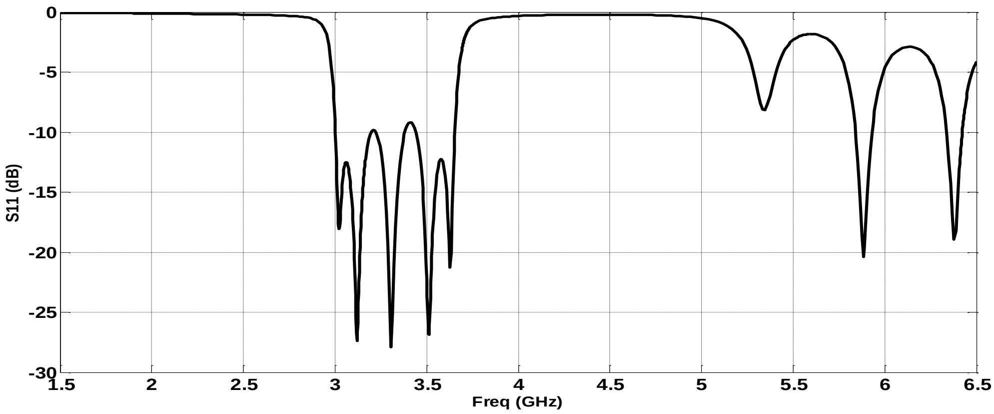


Figure 3.17: Layout of the hairpin filter with $f_o = 3.34$ GHz on Rogers 6010 substrate.

Compared to the previous parallel CL filter designed for the same frequency range with its first spurious response edge at 6.04 GHz, the first spurious response of the hairpin filter starts at 5.3 GHz with higher amplitude. The amplitude of this spurious response was around -10 dB for the CL filter whereas it increased to approximately -2 dB for the new hairpin filter. Hence, the conventional parallel CL filter exhibits better performance in terms of the spurious response compared to the optimized hairpin filter.



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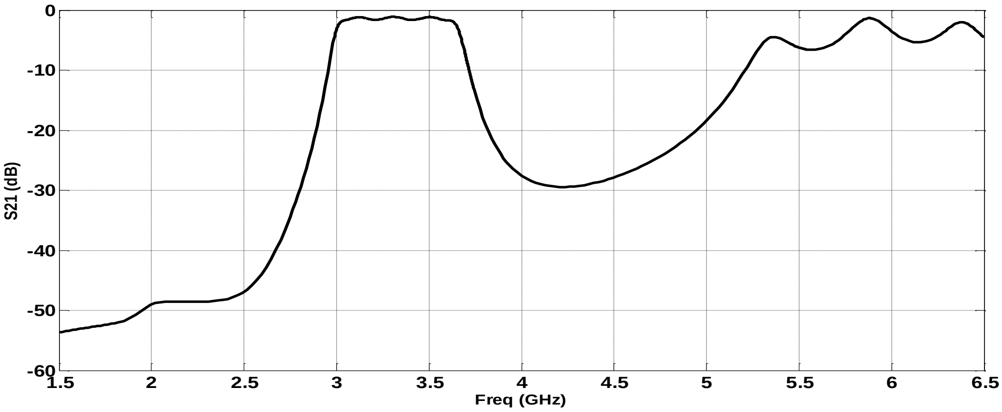

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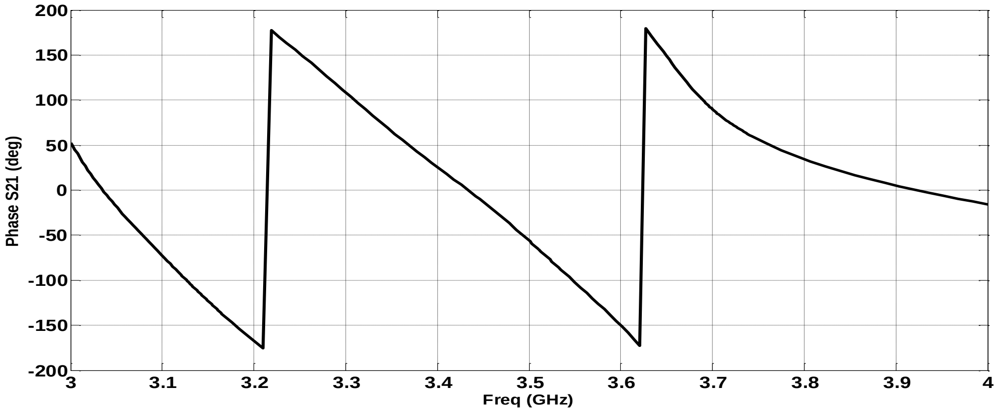


(c)

Figure 3.18: EM response of the optimized hairpin filter with $f_o = 3.34$ GHz (a) S11 magnitude (b) S21 magnitude (c) S21 phase.

3.7.2 Hairpin Filter (3.8-4.4 GHz)

The design and optimization of a hairpin BPF with a center frequency of 4.1 GHz and bandwidth of 3.8-4.4 GHz is similar to the previously designed filter. The equivalent parallel CL filter was designed for a 4.1 GHz center frequency and 16% fractional bandwidth (3.795-4.405 GHz). The overall area of the CL filter was found to be $47.698 \times 13.726\,\text{mm}^2$. In order to prepare for the equivalent hairpin configuration, the optimization was applied as follows: initially, the lengths of all stages were kept the same. Then, the spacing between the coupled line stages was reduced to get a higher coupling and compensate for the distracted coupling due to the reduced resonators' lengths. Accordingly, *b* variables were optimized to reach the desired bandwidth. Finally, the widths and lengths of all resonators were tweaked to set the center frequency of the filter to the desired value.

Similar to the previous hairpin filter, the actual bandwidth of the filter in the EM simulation was reduced compared to the bandwidth of the filter in the schematic simulation. The final optimized dimensions of the hairpin structure with a center frequency of 4.1 GHz using a Rogers 6010 substrate are presented in Table 3.8 below.

Table 3.8: Specifications of the optimized hairpin BPF ($f_o = 4.1\ GHz, \Delta = 0.16$) on Rogers 6010 substrate.

n	$W_n(mm)$	$S_n(mm)$	$L_n(mm)$	$b_{n,n+1}(mm)$
1	0.705	0.161	5.703	0.335
2	0.991	0.411	5.703	0.219
3	0.926	0.599	5.703	0.220
4	0.926	0.599	5.703	0.219
5	0.991	0.411	5.703	0.335
6	0.705	0.161	5.703	NA

Figure 3.19 represents the layout of the filter with the specified dimensions in Table 3.8. The generated mesh in the full-wave EM simulation is obvious on the simulated layout of the filter. This filter is to be utilized as the second filter of the LO channel in the radar system. The size of the hairpin filter is $24.922 \times 9.497\ \mathrm{mm}^2$. Compared to the initially-designed parallel CL filter ($47 \times 14\ \mathrm{mm}^2$), a 63.85% reduction in the overall size of the filter is achieved by the hairpin configuration.

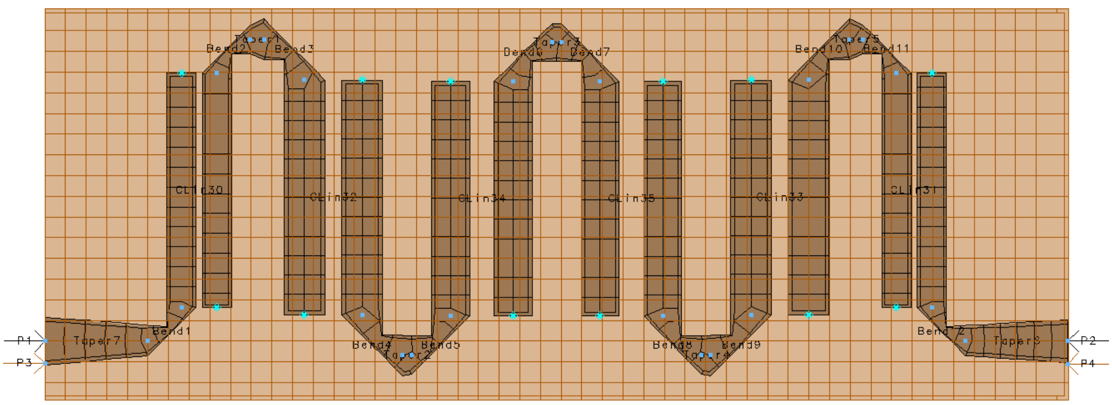
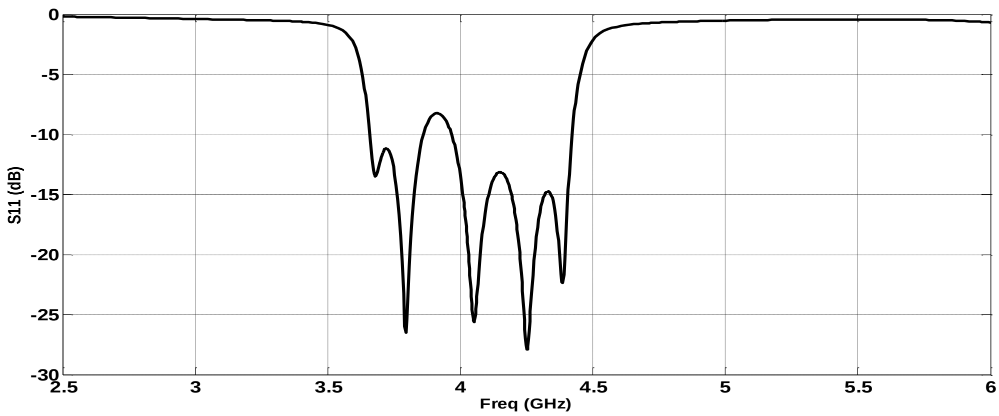


Figure 3.19: Layout of the hairpin filter with $f_o = 4.1$ GHz on Rogers 6010 substrate.

Figure 3.20 shows the return loss, insertion loss, and S21 phase responses of the filter obtained from the EM simulation. From the S21 results of the EM simulation, the bandwidth of the filter is 3.755-4.4 GHz which is the desired bandwidth for the second BPF of the LO channel. The insertion loss over the pass band is better than -1.85 dB. The attenuation level of better than -20 dB is achieved for frequencies of less than 3.542 GHz and those of higher than 4.63 GHz in the stop band. The return loss response verifies a good impedance matching over the entire pass band, as the S11 magnitude is below -10 dB except for a small range of frequencies. The S21 phase response of the hairpin filter is linear over the entire pass band indicating a constant delay for all of the frequency components within the pass band of the filter.



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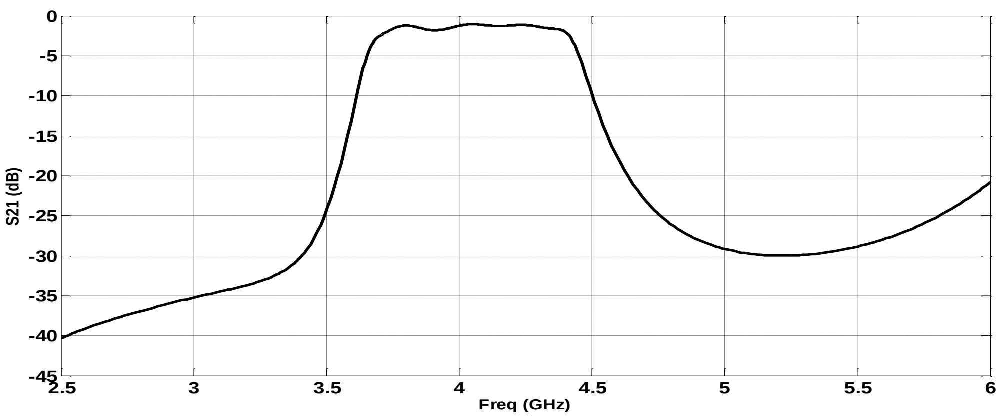

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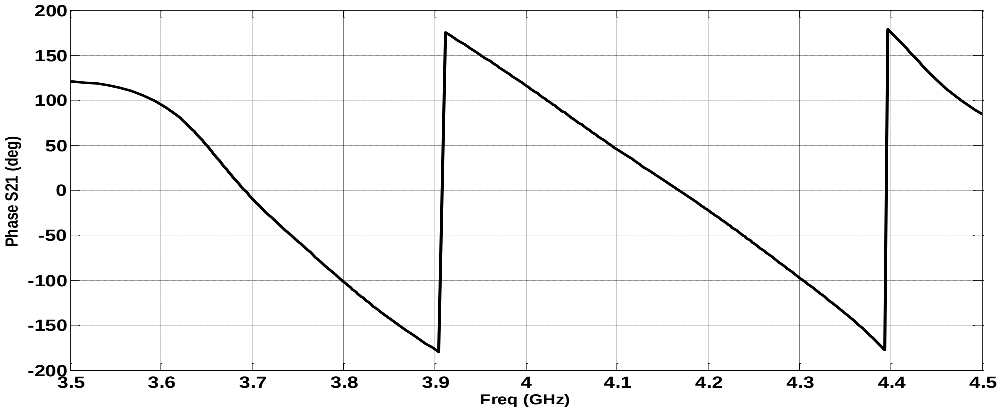


(c)

Figure 3.20: EM response of the optimized hairpin filter with $f_o = 4.1$ GHz (a) S11 magnitude (b) S21 magnitude (c) S21 phase.

3.8 Harmonic Suppression of Microwave Filter Structures

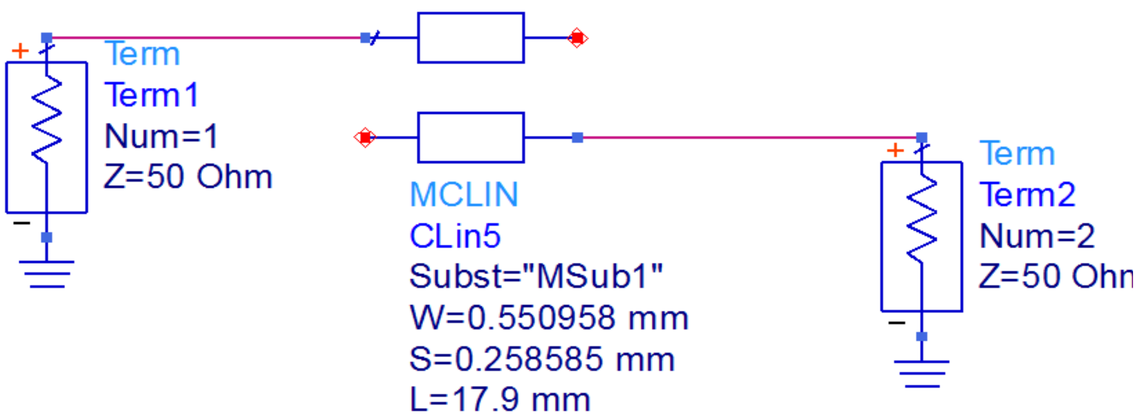
Although the coupled line and hairpin filters offer the advantages of simplicity and low fabrication cost, they suffer from the spurious responses which appear in the stop band. The response of these filters is such that the filter is unable to reject the harmonics of the fundamental frequency band (usually the desired band in which the filter is designated to operate at) [54]. The appearance of the second harmonic $(2f_o)$ in the pass band of these filters is due to the significant difference between the phase velocities of the even- and odd-modes in the specified media. This difference in the phase velocity is due to the large discrepancy of the even- and odd-mode effective dielectric constants of the coupled microscrip lines [55]. The magnitude of the second harmonic is more significant if a substrate with higher permittivity is used due to the larger deviation in the phase velocities. Hence, the second harmonic of the filters can be rejected by equalizing the two different velocities.

Several methods for the compensation of the phase velocity difference in the even- and odd-modes for harmonic suppression of the microwave filters have been presented in the literature [56-63]. Loading the open ends of the filter with open-circuited stubs, SIRs, the use of fractal geometries, substrate suspension, over-coupled stages and defected ground structures are among these methods.

3.8.1 Over-Coupled Resonators

This method is used for the parallel CL filters in which the coupled lines are allowed to overlap more than the resonator proper [64]. Two types of over-coupled resonators are used for the parallel CL filters: in the first type, called end-stage over-coupled resonators, only the length of the first and the last CL stages are extended while in the second type, all the coupled stages are over-coupled. While the latter type is capable of reducing the amplitude of multiple spurious bands [65], the first type presented in [66] is only capable of rejecting the second harmonic. The effectiveness of this method was examined on a third-order parallel CL Chebyshev BPF with 0.1 dB ripples designed on a Rogers 6010 laminate. The center frequency of the filter was chosen to be 2 GHz with a 20% fractional bandwidth.

The over-coupled stages are achieved by increasing the lengths of the CL resonators. This increase in the length is done such that a zero is placed at the second harmonic of the filter's center frequency. Figure 3.21 (a) shows a pair of coupled lines with $W = 0.551$ mm and $S = 0.259$ mm, the same as the calculated width and spacing for the first and last stages of the filter. The length of the resonators was found to be 17.9 mm in order to have a null at 4 GHz, which is the second harmonic of the filter's center frequency. Figure 3.21 (b) depicts the layout response of this CL stage. As is seen in the plot, a null is located at 4 GHz in the S21 response of the filter. This null could be utilized in order to eliminate the second harmonic of the CL BPF. In addition, the S11 response of the single stage close to this frequency band is around 0 dB, indicating a full reflection of the signals at these frequencies.



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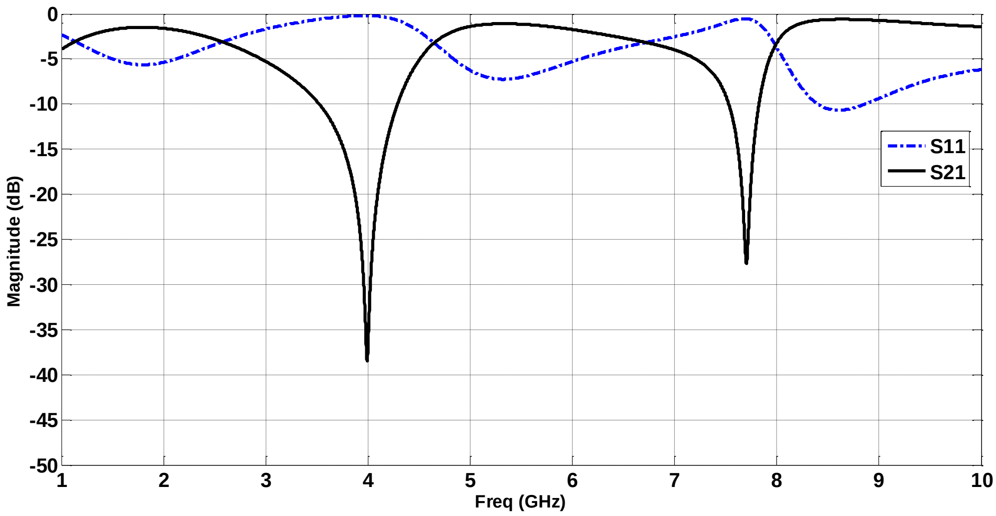


(b)

Figure 3.21: Single stage parallel CLs (a) ADS Schematic (b) S-parameter responses.

The original length of the first stage was calculated to be 15.174 mm, while the length of the resonators should be 17.9 mm in order to attain a null at 4 GHz. Hence, the first stage should be extended by $\theta_1 = 2.726$ mm (corresponding to $\theta_1 = 13.359°$ at 2 GHz) which is the required length difference. The required extension in the length of the last stage (θ_2) was found with the help of the ADS optimization. A length difference of $\theta_2 = 1.5$ mm corresponding to $\theta_2 = 7.350°$ at 2 GHz was found to be optimum for the last stage to achieve the best suppression at 4 GHz. Equation (3.4) relates the physical length (in m) to the electrical length (in degrees), where c is the speed of light. The layout of the end-stage over-coupled BPF is shown in Figure 3.22.

$$l = \frac{\theta\, c}{2\pi f\sqrt{\varepsilon_{eff}}}\left(\frac{\pi}{180}\right) \tag{3.4}$$

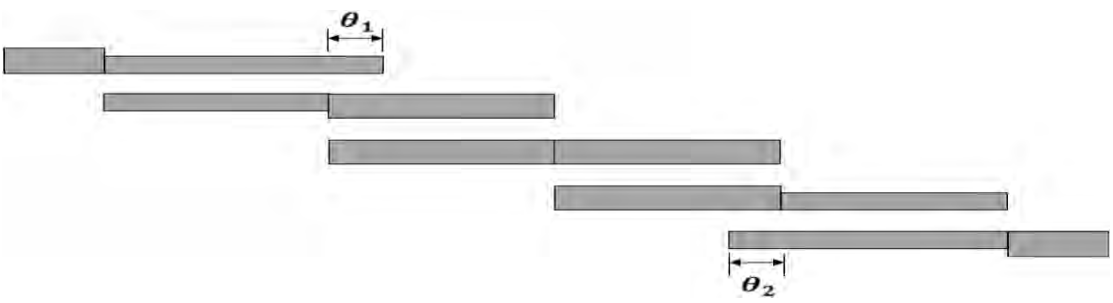
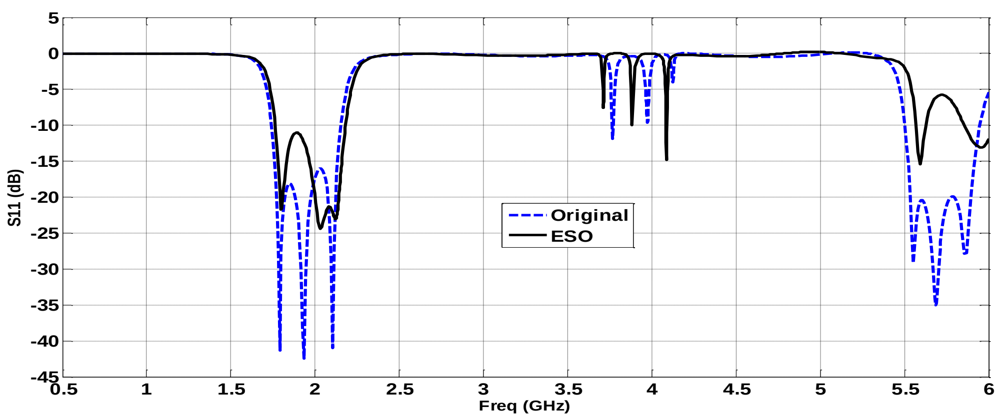


Figure 3.22: Layout of designed parallel CL BPF with end-stage over-coupled.

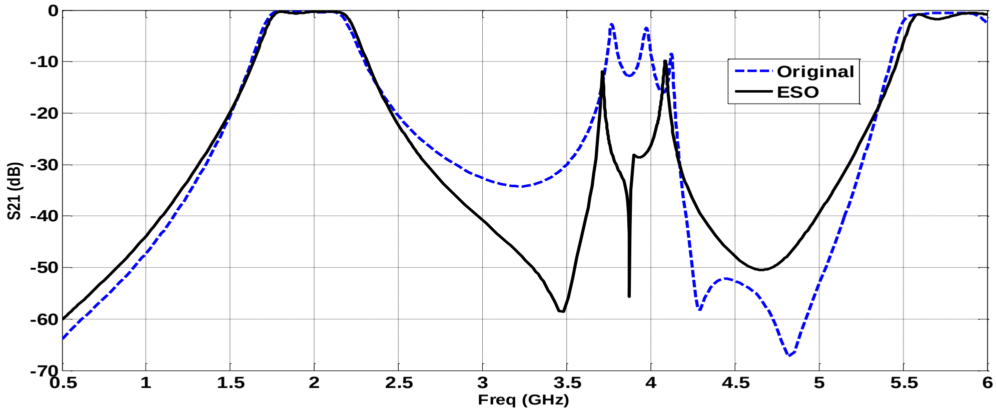
Figure 3.23 compares the response of the original CL BPF along with the end-stage overlay fashion. Although the S11 response of the filter is influenced by the over-coupled stages, it is below the standard -10 dB in the filter's pass band indicating an acceptable impedance matching between the filter and the 50 Ω characteristic impedance of the system.

While the S21 response of the filter is not changed over the pass band, the amplitude of the first spurious response is reduced to less than -10 dB. This indicates proper suppression of the second harmonic without additional distortion in the filter's pass band. A better rejection of 28 dB is achieved at 3.5 GHz as the magnitude of S21 is reduced to -58 dB from -30 dB in the original filter response. Although the magnitude of S21 is below -10 dB over the entire band of the first spurious response, the end-stage overlay is not completely successful in rejecting the lower and upper frequency edges of this band. This is due to the use of a substrate with a high dielectric constant which results in a high difference between the even- and odd-mode phase velocities. The S21 magnitude is above -20 dB for the two frequency edges which are 3.71 GHz and 4.09 GHz. In addition, the second spurious band at the third harmonic of the fundamental pass band is not affected by this method. Hence, the over-coupling of all stages is a solution in order to completely eliminate the first and second spurious bands for this substrate.

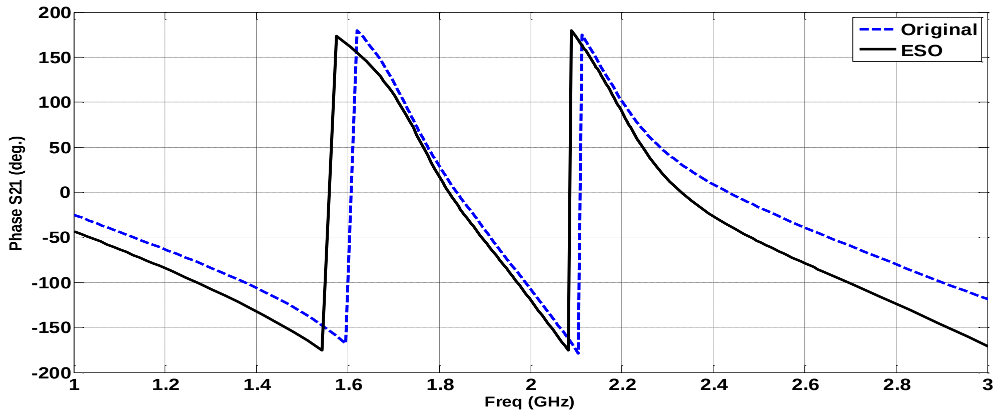
As shown in the comparison plot of the S21 phase, the phase of the over-coupled filter is linear over the filter's pass band with minimal changes with respect to the S21 phase response of the original filter.



(a)



(b)

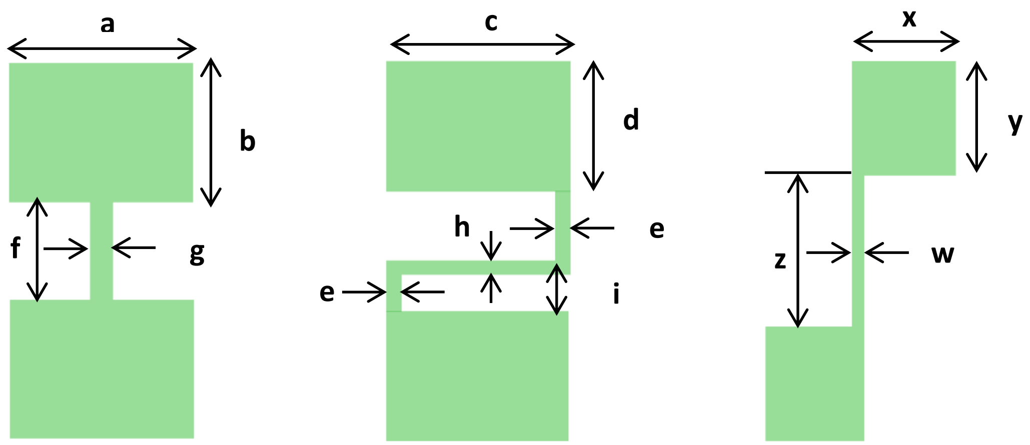


(c)

Figure 3.23: Comparison between EM responses of conventional parallel CL BPF vs. over-coupled version (a) S11 magnitude (b) S21 magnitude (c) S21 phase.

3.8.2 Defected Ground Structure

The most common method for the harmonic suppression used in the literature is defected ground structure (DGS). DGS is a technique in which the ground plane is deliberately modified to improve the stop band characteristic of the filter [67]. In this technique, artificial structures (periodic or non-periodic) are etched into the ground plane which results in changing the inductance and the capacitance of the structure [68]. Several geometries such as dumbbell, rectangular, square head, circular head, arrow head slot, fractal, spiral, L-shaped, U-shaped , V-shaped, and interdigital have been reported in the literature [69-71]. The superiority of the DGS technique over the other suppression techniques is that it can be used for any type of microstrip filter. Figure 3.24 represents three different shapes which are examined in this study to suppress the second harmonic of the designed BPF. The optimized dimensions are provided below each structure.



(a) (b) (c)

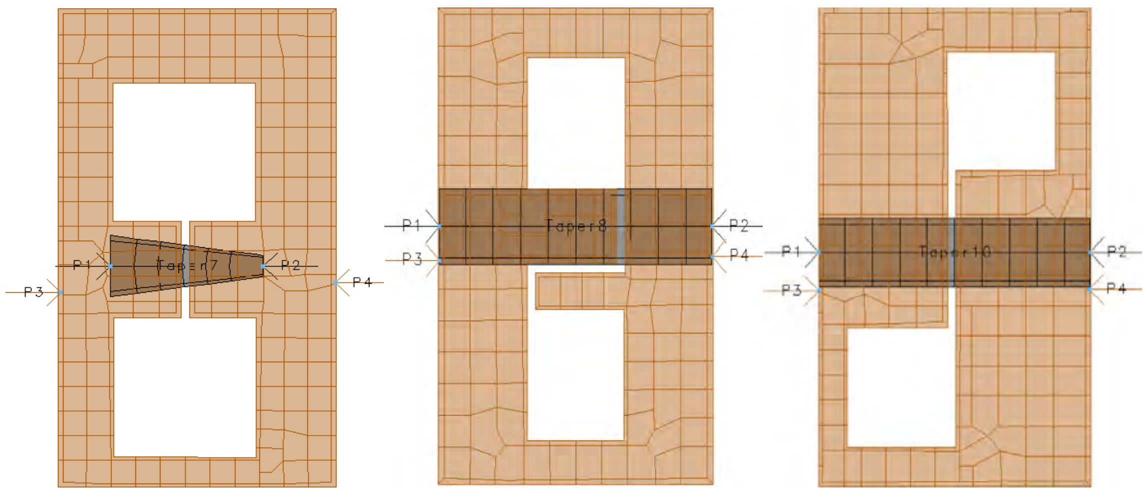
Figure 3.24: Utilized DGSs (a) Dumbbell (b) Flip-S (c) Flip-Z.

a = 2.60 mm b = 2.60 mm g = 0.15 mm f = 1.82 mm	c = 1.80 mm d = 2.00 mm e = 0.15 mm h = 0.15 mm i = 0.55 mm	x = 2.00 mm y = 2.00 mm w = 0.15 mm z = 2.63 mm

The distribution of the shield current in the ground plane is changed by these ground plane defects which enable the EM waves to penetrate through the substrate to the ground at the resonance frequency of the structure. Hence, each DGS structure can be modeled as a parallel RLC resonator circuit which acts as an open circuit at its resonant frequency [72, 73]. This property can be used by the appropriate selection of DGS structure and its dimensions to filter the spurious responses of the half-wave resonator filters.

Figure 3.25 shows the simulated DGSs along with a 50 Ω microstrip line with width $W = 1.156\,\text{mm}$ on a Rogers 6010 substrate. The comparison results of these simulations are shown in Figure 3.26. These geometries are aimed to be used for the designed hairpin filter with a center frequency of 3.34 GHz and a 3.02-3.66 GHz pass band.

In Figure 3.26, the dumbbell, flip-S, and flip-Z structures are labeled as DGS1, DGS2, and DGS3, respectively. As inferred from the S11 responses, DGS2 offers the best reflection coefficient over the center frequency and pass band of the filter. The dimensions of these structures were optimized such that the null of the S21 response is placed at 6 GHz for DGS1, slightly higher than 6 GHz for DGS2, and slightly lower than 6 GHz for DGS3. The insertion loss of all three DGS structures is very low and negligible over the filter's pass band.



(a) (b) (c)

Figure 3.25: Simulated DGSs with 50 Ω microstrip line on a Rogers 6010 substrate (a) Dumbbell (b) Flip-S (c) Flip-Z.

After examining the response of the individual DGS structures, they were added to the layout of the hairpin BPF and the full-wave EM simulation was performed. For instance, Figure 3.27 represents the layout of the hairpin BPF with the added dumbbell DGS beneath the input feeding microstrip line. The generated simulation mesh is obvious in the figure as well. The mesh frequency was set to 10 GHz and the mesh density was specified to 30 cells per wavelength for these simulations.

The comparison between the BPFs' responses with different DGS structures along with the conventional hairpin filter is shown in Figure 3.28. As was expected from the S11 response comparison of the individual DGS, the best reflection property over the filter's pass band is achieved when DGS2 is added to the hairpin filter layout. While DGS3 offers an acceptable reflection property over the pass band, the offered reflection response of the filter with DGS1 is not acceptable as it is above -5 dB. Hence, this indicates a remarkable reflection over the filter's pass band.

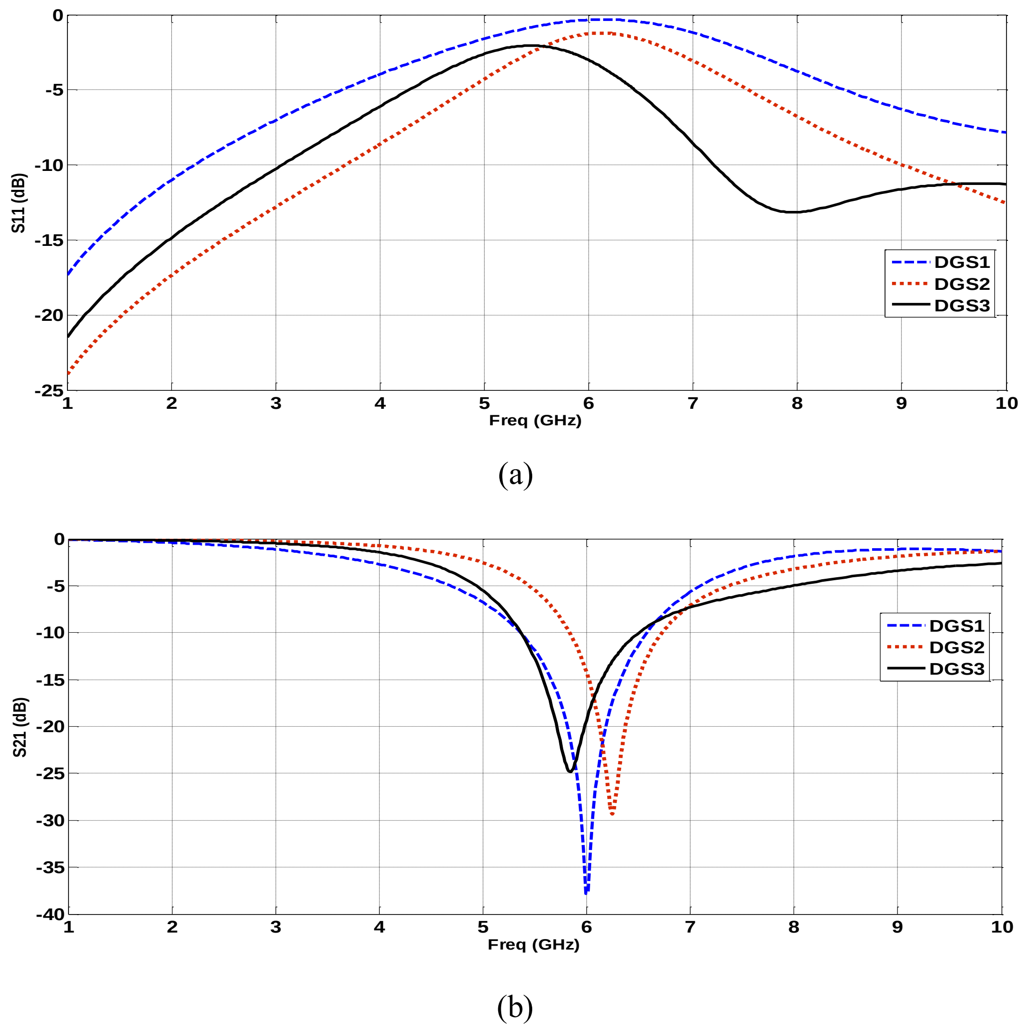


Figure 3.26: EM response of utilized DGSs (a) S11 magnitude (b) S21 magnitude.

Due to improper impedance matching of the filter with DGS1, the ripple and loss of this structure are the worst compared to other DGSs. From the S21 comparison plot, DGS1 offers the best suppression behaviour at the first spurious band (i.e., the second fundamental frequency of the pass band). In addition, DGS3 is successful in suppressing this spurious response to be below -10 dB, whereas DGS2 is not successful in this mission.

In conclusion, DGS2 and DGS3 (flip-S and flip-Z DGS) with the presented dimensions are suitable DGS structures for the designed hairpin BPF with a 3.34 GHz center frequency and fractional bandwidth of 0.192. The dimensions of the dumbbell

DGS should be further optimized to enhance the impedance matching of this structure to 50 Ω. This impedance matching is essential in order to use DGS1 in the layout of the intended filter for harmonic suppression. It is worth noting that the bandwidth of the original filter is not affected by utilizing different DGS structures and the S21 phase response of the filter remains linear in all cases, similar to the conventional hairpin filter.

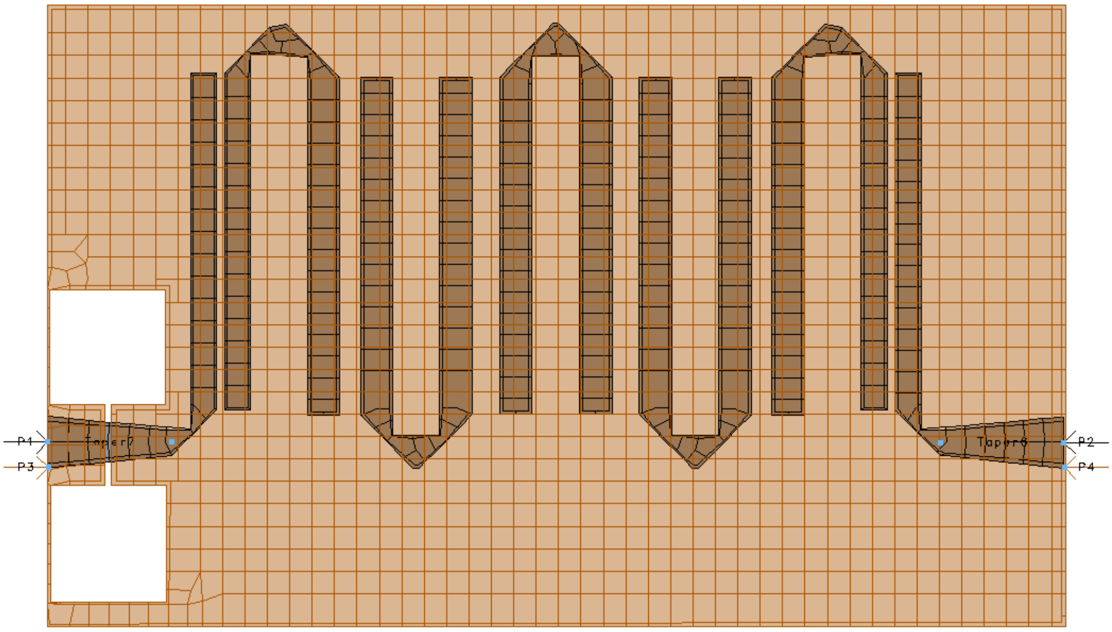
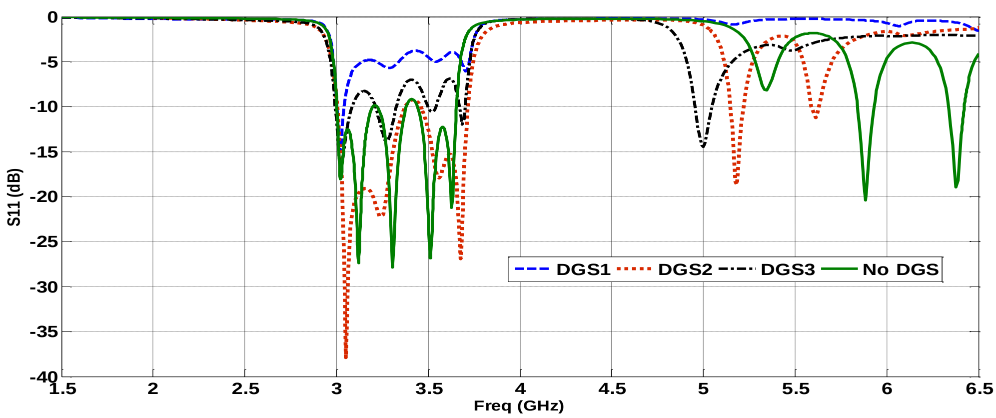


Figure 3.27: Layout of hairpin filter with added DGS (dumbbell shape).



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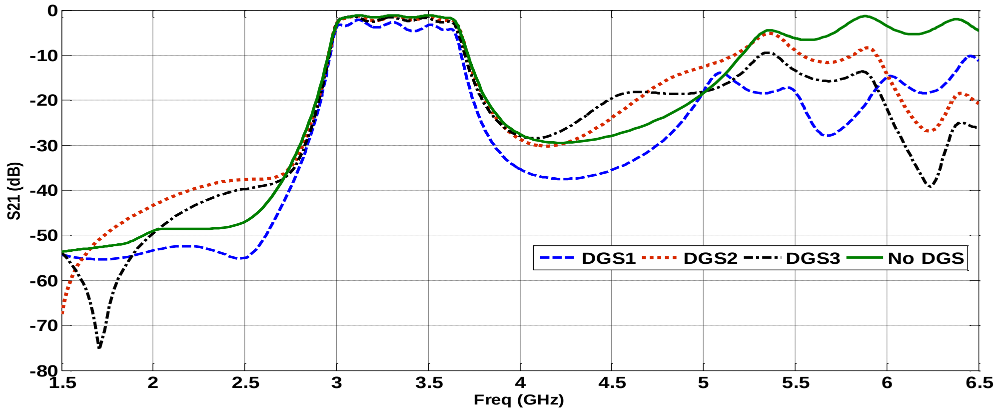

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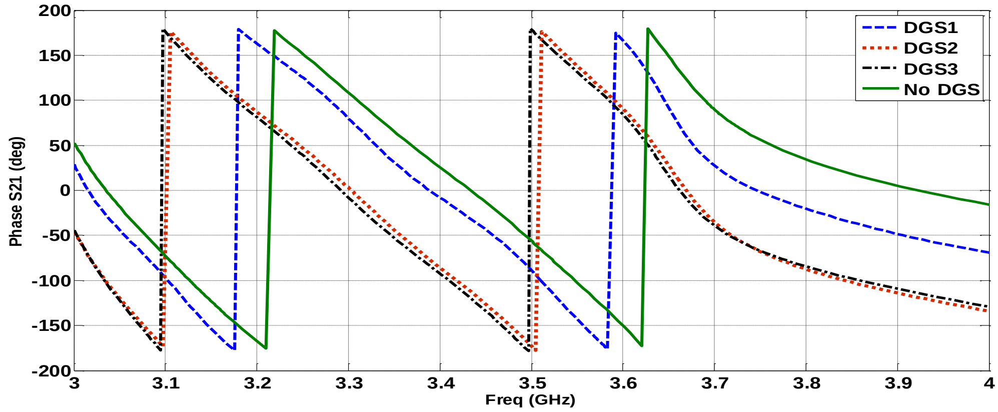


(c)

Figure 3.28: EM response of conventional hairpin BPF vs. different added DGSs (a) S11 magnitude (b) S21 magnitude (c) S21 phase.

3.9 Interdigital BPF

Interdigital filters are created by an array of n quarter-wavelength transmission line resonators. These resonators are placed next to each other and are short-circuited to the ground from one end and open-circuited from the other end with alternative orientation. The electrical length of these lines is calculated to be 90^0 at the center frequency of the filter's pass band. The detailed design equations of interdigital filters are presented in [74].

The greatest advantage of the interdigital filter structure lies in its compactness, which allows this structure to be easily integrated into chip level applications such as CMOS technology [75]. This compactness is due to the higher coupling factor of the interdigital configuration compared to the parallel CLs which results in better frequency performance as well [76]. Another advantage of this filter structure is its inherent suppression of the first spurious resonant frequency (at $2f_o$) which is a major advantage of interdigital filters over other microwave filters such as parallel CLs and hairpin filters. This inherent suppression of the second harmonic resonant frequency is due to the utilization of a grounded quarter-wavelength-long resonator which pushes the first spurious response of the filter to occur at around three times of the fundamental resonant frequency [77]. Moreover, the third harmonic of the filter pass band can be suppressed with the under-coupled technique of the quarter-wavelength resonator pairs presented in [78]. The under-coupled technique is simple and is achieved by shifting one of the resonators towards the propagation direction, which greatly enhances the stop band characteristic of the interdigital filter.

One of the drawbacks of the interdigital filter is the required groundings at either end of the resonators. These groundings are done through vias, which connects two conductive layers of the PCB through a hole created in the substrate. The utilization of these grounding vias increases the design complexity due to the added inductors, in addition to the increase in the fabrication cost. Furthermore, a proper modeling of the vias during the design and simulation phases of the filters is vital to prevent a significant frequency shift in the response of the fabricated filter [79]. Another drawback of the interdigital filter is that filters with very high fractional bandwidths cannot be realized easily due to the high required couplings between the adjacent resonators in such filters [80]. The coupling between the adjacent resonators in such microstrip filters is limited by the fabrication limitations on the minimum allowable space between them.

Interdigital filters were chosen for the first filters of the TX and LO channels as they are intended to reject the higher side band of the mixer product. The design, optimization, and simulation of the two interdigital filters for 1.52-1.82 GHz (TX channel) and 1.9-2.2 GHz (LO channel) are discussed in the following section. The proper modeling of the interdigital filters with vias is done using the full-wave EM simulator of ADS (Momentum). It is noted that vias with 0.3302 mm (13 mils) diameters are used in the EM simulations of the interdigital filters presented in the following section.

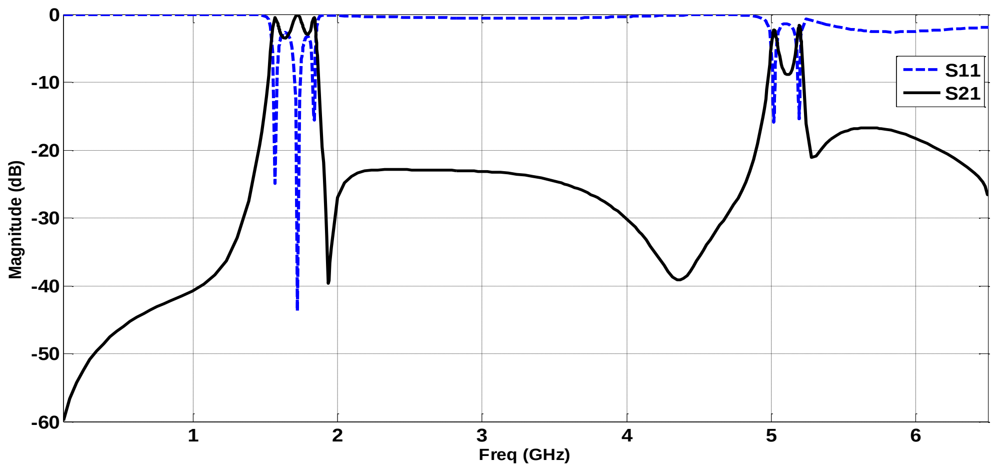
3.9.1 Interdigital Filter (1.52-1.82 GHz)

Several interdigital filters were designed to be implemented on a Rogers 6010 laminate with a thickness of 1.27 mm. It was found that if a 150 MHz offset in the center frequency of the filter was considered at the design stage, the full-wave EM simulation response of the filter would be closer to the desired band. In addition, the bandwidth of the filters in the EM simulation is reduced compared to the designated one. Hence, for the initial design, a fifth-order Chebyshev BPF with 0.2 dB ripples was designed initially. The center frequency of the filter was chosen to be 1.82 GHz with a 24% fractional bandwidth. The elements of the normalized LPF prototype were extracted from the standard tables ($g_o = 1$, $g_1 = 1.3394$, $g_2 = 1.337$, $g_3 = 2.166$, $g_4 = 1.337$, $g_5 = 1.3394$, and $g_6 = 1$) and the even- and odd-mode characteristic impedances of all five stages were calculated. Consequently, the physical parameters of each stage were calculated using LineCalc. The electrical lengths of all the stages were $\theta = 90°$ to result in quarter-wavelength resonators. Table 3.9 presents the calculated design parameters of the interdigital filter using a developed MATLAB code. In addition, the position of the tapping line (θ_t) was calculated to be 24.726° which results in an equivalent physical length of 4.387 mm.

The widths and lengths of all stages were approximated to 1.08 mm and 15.9 mm in the simulation. Figure 3.29 shows the layout response of the designed interdigital filter. The simulated center frequency of the filter is 1.69 GHz with a bandwidth of 1.552-1.85 GHz. Although the higher frequency of the pass band is as desired, its lower edge frequency is higher than the desired point. Hence, the lower side of the pass band should be shifted to lower frequencies in order to reduce the attenuation at 1.52 GHz. This shift in the bandwidth helps in shifting the center frequency to the desired point as well. As inferred from the S21 plot, the insertion loss is not flat over the pass band of the filter which causes the group delay of the filter to increase. This results in a distortion in the linearity of the phase response, as shown in Figure 3.29 (b).

Table 3.9: Specifications of fifth-order, 0.2 dB ripple Chebyshev interdigital BPF (f_o =1.82 GHz,$\Delta = 0.24$).

n	$Z_{oe}(\Omega)$	$Z_{oo}(\Omega)$	$W(mm)$	$S(mm)$	$L(mm)$
1,2	58.141	43.859	1.066	1.339	15.967
2,3	56.187	45.041	1.089	1.674	15.915
3,4	56.187	45.041	1.089	1.674	15.915
4,5	58.141	43.859	1.066	1.339	15.967



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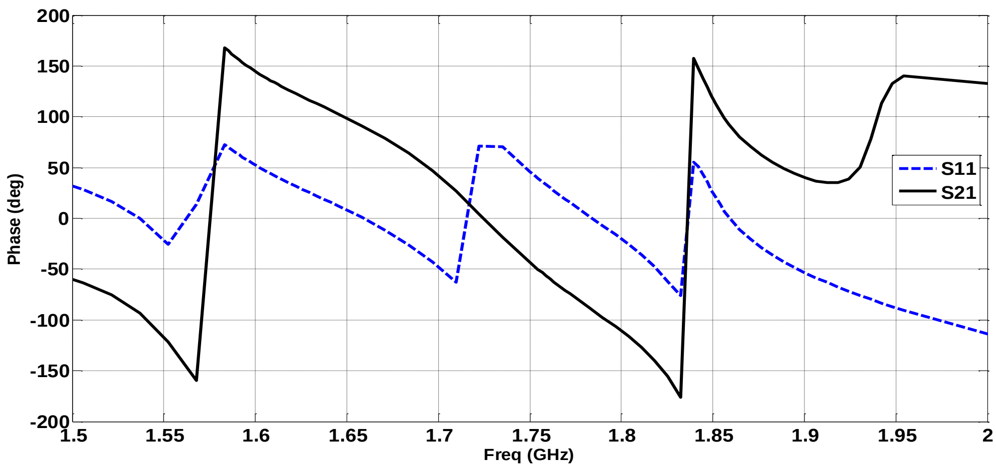


(b)

Figure 3.29: EM simulation responses of the designed interdigital filter (a) Magnitude (b) Phase.

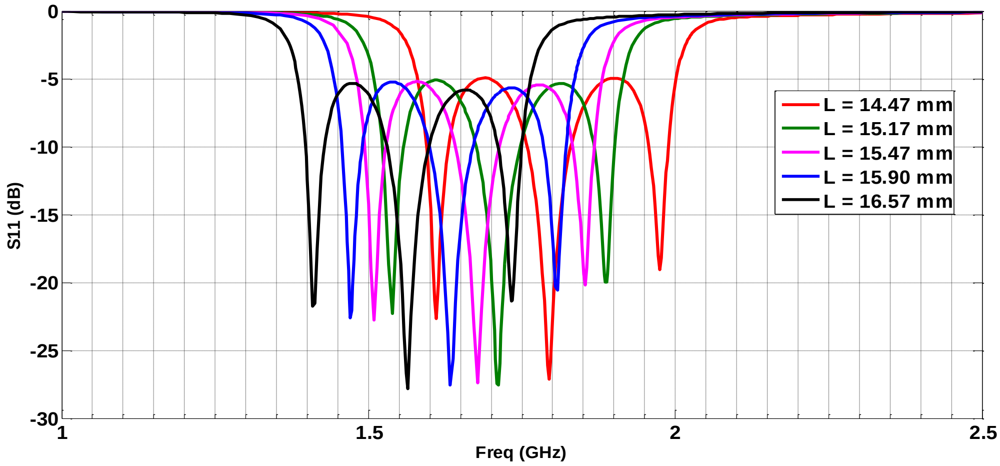
The reflection coefficient of the filter over the pass band is not optimal. The reason for having a large reflection over the pass band is due to improper impedance matching between the source impedance (50 Ω) and the input impedance of the filter. This is inferred from the S11 response as it is not below the standard -10 dB, indicating that a considerable portion of the signal power is reflected back towards the feed line port rather than transferring to the second port of the filter. Hence, proper optimization of the dimensions helps in enhancing the reflection coefficient which simultaneously results in flattening the insertion loss of the filter as well. The effect of different parameters on the overall response of the filter is discussed in the next section.

3.9.1.1 Interdigital Filter Optimization

The effect of different parameters in the layout of the interdigital filter was examined in order to shift the center frequency of the filter and enhance the impedance matching. Hence, different parameters of the filter such as the length of the resonators, the spacing between the outer and inner resonator stages, the resonators' widths, the position of the tapping line, the overall length of the input/output resonators, and the width of the feed lines were swept to observe the overall effect.

3.9.1.1.1 Effect of the resonators' length (Ln)

The lengths of all resonators were swept from 14.47 mm to 16.57 mm and the layout of the filter was simulated using the Momentum simulator of ADS. The S11 and S21 responses of the filter with different resonators' lengths are plotted in Figure 3.30. As shown, the total length of the resonators affects the center frequency of the filter without significantly altering other filter specifications such as bandwidth, insertion loss fluctuations, and return loss. The center frequency of the filter shifts to a lower frequency by the increase in the total length of the resonators.



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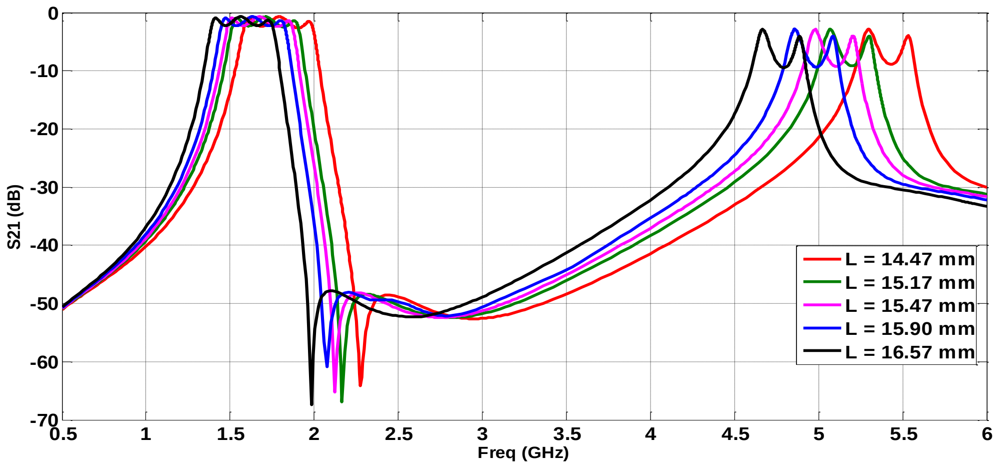
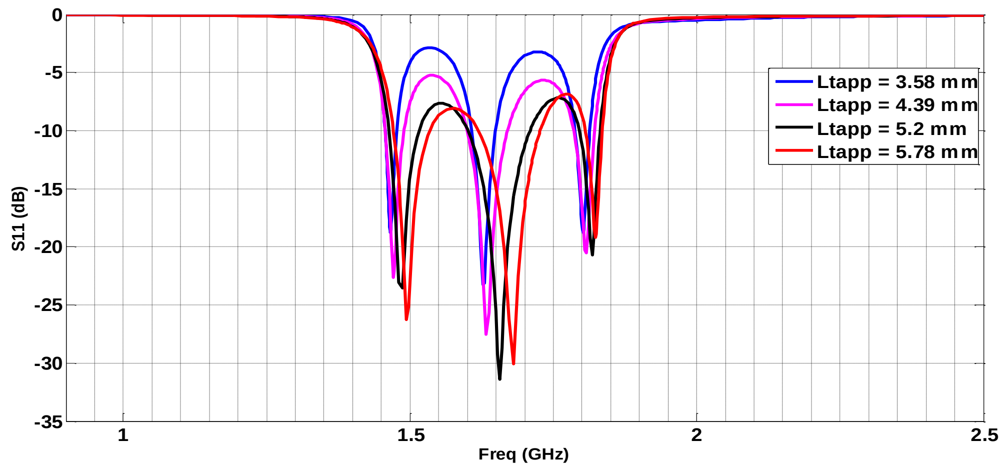


(b)

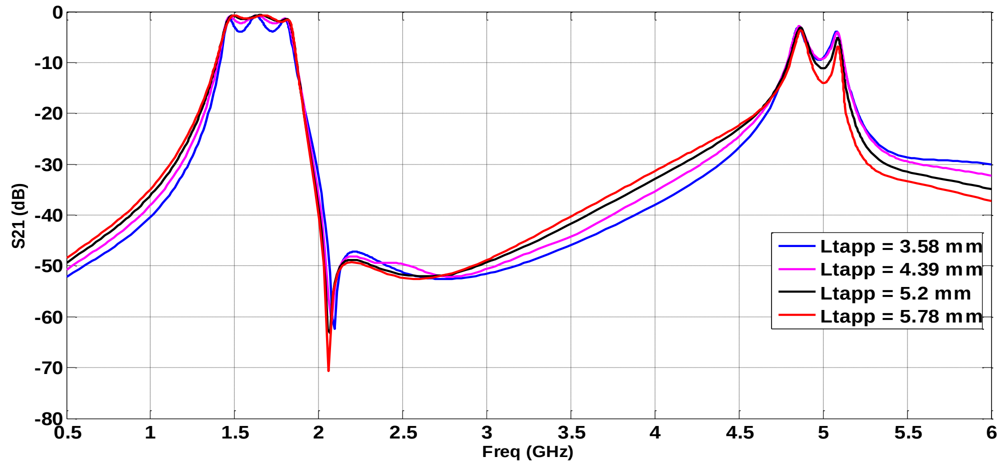
Figure 3.30: Effect of the resonators' length on the interdigital filter response.

3.9.1.1.2 Effect of the tapping position (θ_t)

It was observed that the position of the tapping line is critical in the impedance matching of the filter and the source. Hence, the location of the feed point to the interdigital filter impacts its return loss response as well as the pass band's ripples.



(a)



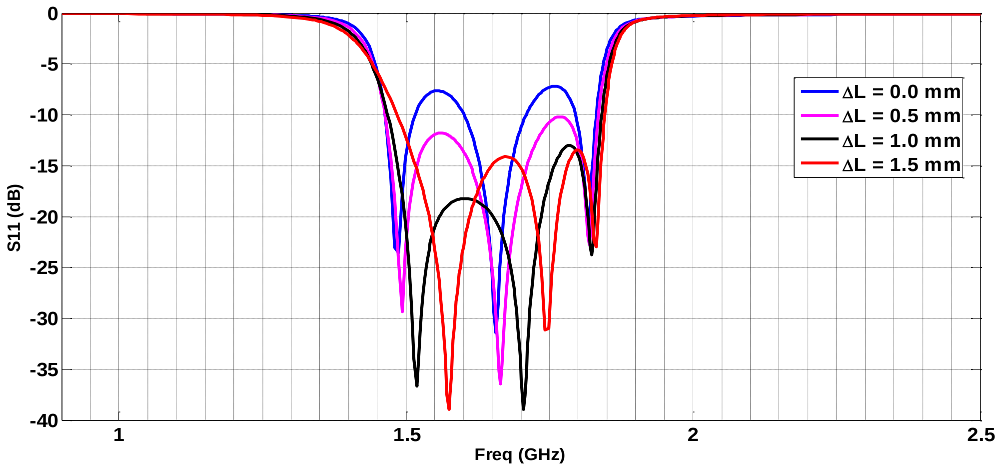
(b)

Figure 3.31: Effect of the tapping position on the interdigital filter response.

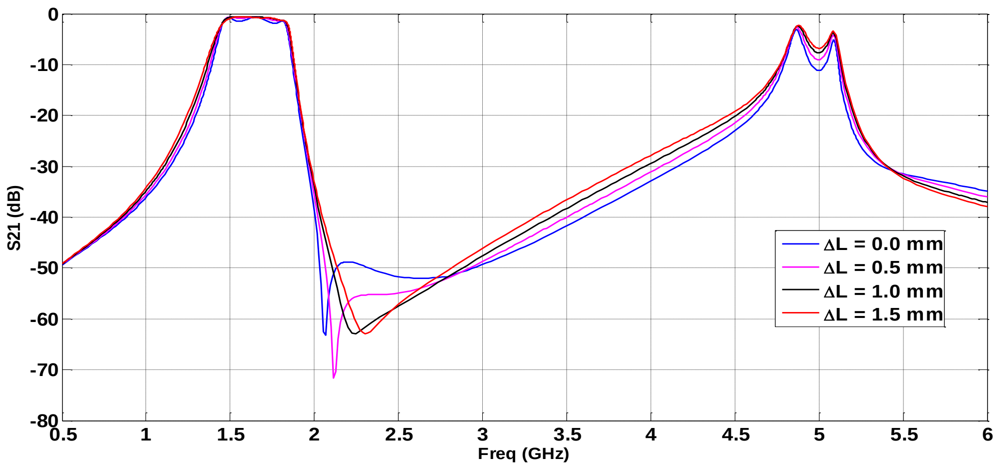
The response of the filter was monitored by varying the position of these tapping lines at the two ports of the filter. This parameter was swept from 3.58 mm to 5.78 mm and the simulation results are shown in Figure 3.31. From the sweep comparison results, it is concluded that the return loss is improved by increasing the tapping position. In addition, the insertion loss of the filter is reduced which, in turn, leads to a flatter response due to the enhanced impedance matching over the filter's pass band. Furthermore, the impedance matching of the filter is not significantly improved as the difference between the filter's responses for the tapping positions of 5.2 mm and 5.78 mm is minimal. Hence, a tapping distance of 5.2 mm is optimal for the desired interdigital filter. It is worth noting that the effect of the tapping position on the center frequency and bandwidth of the filter is insignificant.

3.9.1.1.3 *Effect of the input/output resonators length ($\Delta L_1, \Delta L_n$)*

In all the previous simulations, the lengths of all resonators were equal ($\Delta L = 0$). While optimizing the return loss of the interdigital filter, it was found that the return loss response of the filter could be further enhanced by a further increase in the lengths of the I/O resonators (L_1 and L_5).



(a)



(b)

Figure 3.32: Effect of the I/O resonators' lengths on the interdigital filter response.

Figure 3.32 represents a comparison between the responses of the same interdigital filter with different increases in the lengths of the I/O resonators. As shown in the plots, the return loss is pushed to be better than -10 dB as the length of these two resonators is increased compared to the lengths of the other stages. Due to the enhanced impedance matching, the insertion loss is smoother (flattened) over the entire pass band. Moreover, the amount of loss in the filter is further reduced, as can be seen from the S21 response. From the shown parametric results, it is concluded that a 1 mm increase in the lengths of the I/O resonators compared to the other stages results in the best return loss and insertion loss of the desired interdigital filter.

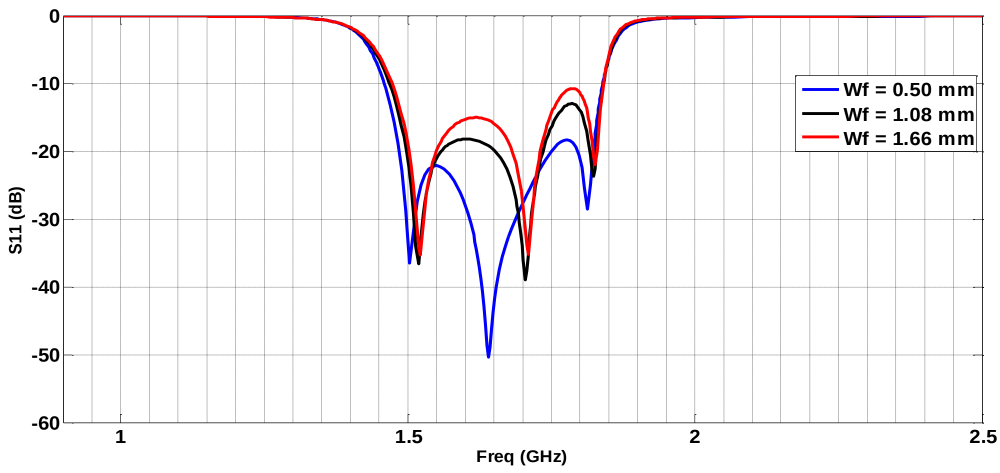
3.9.1.1.4 Effect of the feed line's width (W_f)

In all previous simulations, the widths of the feed lines were equal to the widths of the resonators (1.08 mm). It was shown that by changing the position of the tapping line as well as increasing the lengths of the I/O resonators, the impedance matching is enhanced. Another factor in such impedance matching is the width of the microstrip feed lines in order to further enhance the impedance matching and subsequently, the return loss. Hence, the filter was fed by microstrip lines of different widths of 0.5 mm, 1.08 mm, and 1.66 mm. Figure 3.33 depicts a comparison of the filter response when it is fed using different microstrip lines with different impedance levels. While the change in the S21 response is minimal by altering the width of the feed lines, the S11 response is greatly improved when the filter is fed with microstrip lines of 0.5 mm widths. The return loss of the filter over the pass band is better than -20 dB which ensures minimal reflection and maximum transmission of the signal's power to the other port of the filter at the pass band frequencies.

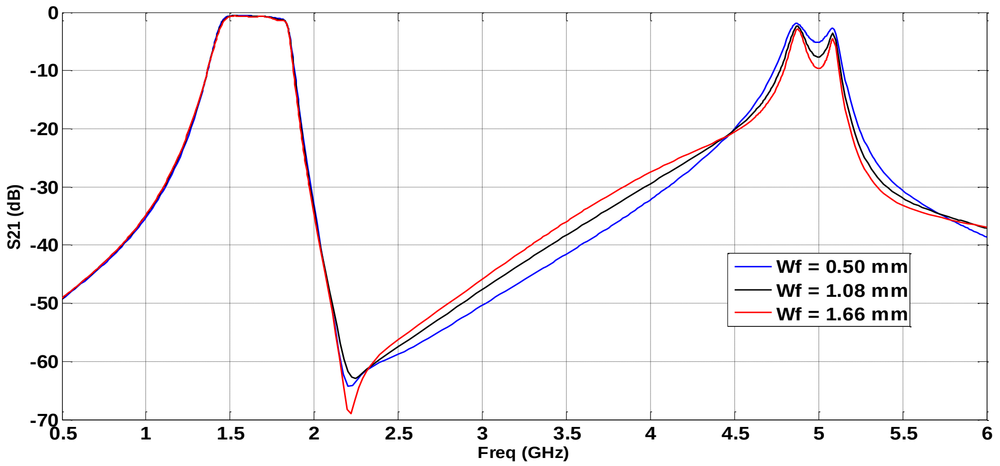
3.9.1.1.5 Best combination

Table 3.10 summarizes the final dimensions of the optimized interdigital BPF to be fabricated for the TX channel ($f_o = 1.67\ GHz, BW = 300\ MHz$) of the radar testbed. The layout of the optimized interdigital filter is depicted in Figure 3.34. The generated mesh for the Momentum simulator is shown in the figure as well. The brown rectangle on the top of the interdigital structure represents the ground plane. The filter is fed by the two 50 Ω ports shown in black and the according brown ports represent the ground reference points of the ports. The overall size of the filter is 15.6 × 18.8 mm^2.

Figure 3.35 shows the magnitude and phase responses of the optimized final interdigital filter for the TX channel. As is shown, the return loss response of the filter is below -20 dB indicating a good impedance matching of the filter to the 50 **Ω**. The insertion loss of the filter is flat and is minimal over the pass band of the filter. The filter does not exhibit a spurious response at the second harmonic of the filter's pass band where the rejection level is below -40 dB around 3.34 GHz. The phase responses of the filter are linear indicating a constant group delay of the filter over the entire pass band frequencies.



(a)



(b)

Figure 3.33: Effect of the feed line's width on the interdigital filter response.

Table 3.10: Final dimensions (in mm) of the optimized interdigital filter for TX channel (f_o = 1.67 GHz, BW= 300 MHz).

W_f	L_{tapp}	W_n	L_1, L_5	L_2, L_3, L_4	$S_{2,3}, S_{3,4}$	$S_{1,2}, S_{4,5}$
0.5	5.2	1.08	17.68	15.87	1.5	1.06

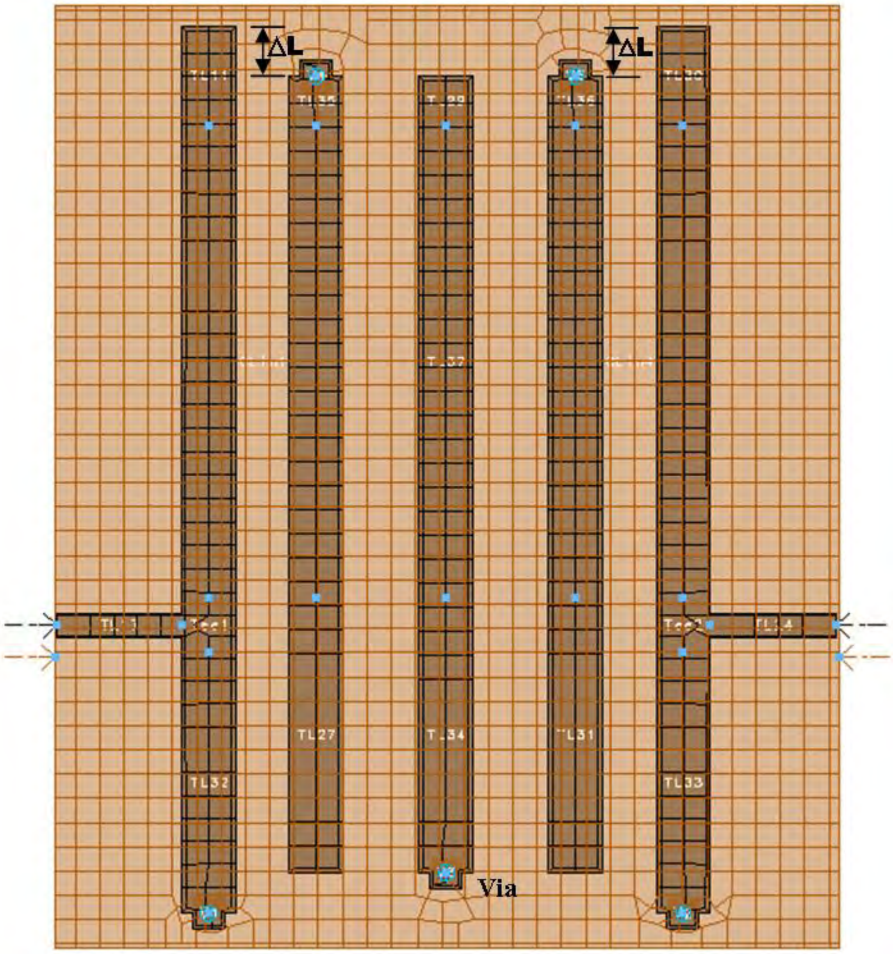


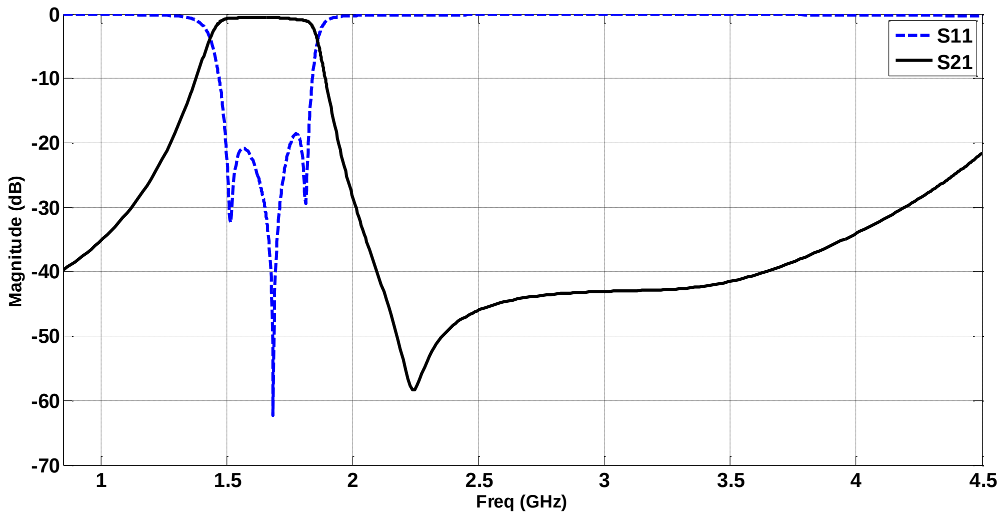
Figure 3.34: Layout of the optimized interdigital filter for TX channel ($f_o = 1.67$ GHz, $BW = 300$ MHz).

3.9.2 Interdigital Filter (1.9-2.2 GHz)

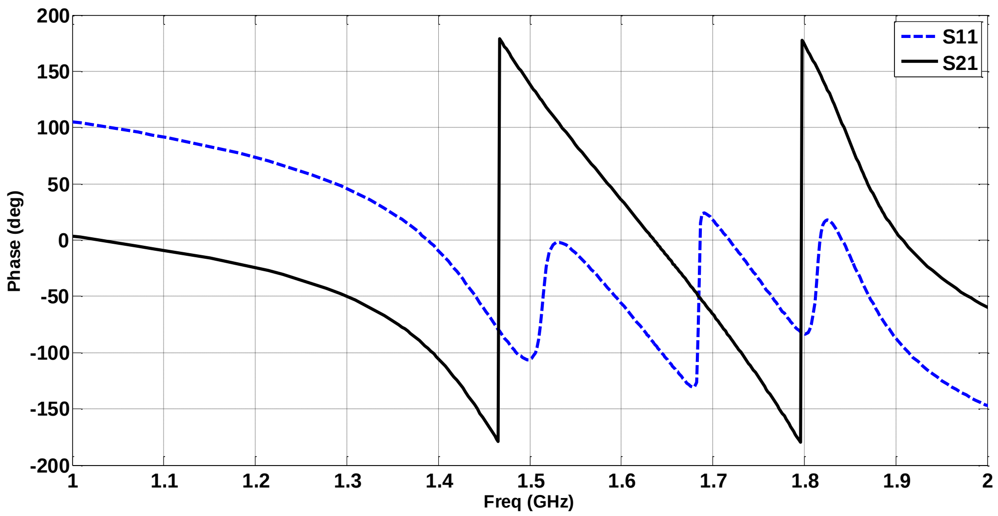
The 150 MHz frequency shift observed in the previous interdigital filter was considered prior to the dimension calculations of the new desired filter. Hence, a design center frequency of 2.2 GHz with the same fractional bandwidth of 24% was chosen for the design calculations of this interdigital filter. Table 3.11 summarizes different design specifications of a fifth-order Chebyshev BPF with 0.2 dB ripples on a Rogers 6010 substrate with 1.27 mm thickness. The position of the tapping line was calculated to be $\theta_t = 24.726°$ which results in a physical electrical length of 3.63 mm for the obtained characteristic impedances of the first and last resonator stages.

It is noted that the values of the even- and odd-mode characteristic impedances are same as those in Table 3.9, as the fractional bandwidth is the same for both filters.

In the simulations, the width and length of all resonators' stages were chosen to be 1.1 mm and 13.1 mm, respectively. The simulation results of the interdigital filter with the obtained dimensions in Table 3.11 are shown in Figure 3.36. Similar comments on the response of the previously designed interdigital filter for the TX channel are applicable for the response of this filter as well. Hence, similar optimization procedures were followed to achieve the desired response.



(a)



(b)

Figure 3.35: EM simulation responses of the optimized final interdigital filter for TX channel (a) S11 and S21 Magnitude (b) S11 and S21 phase.

Table 3.11: Specifications of fifth-order, 0.2 dB ripple Chebyshev interdigital BPF (f_o=2.2 GHz, Δ = 0.24).

n	$Z_{oe}(\Omega)$	$Z_{oo}(\Omega)$	$W(mm)$	$S(mm)$	$L(mm)$
1,2	58.141	43.859	1.067	1.342	13.184
2,3	56.187	45.041	1.089	1.678	13.141
3,4	56.187	45.041	1.089	1.678	13.141
4,5	58.141	43.859	1.067	1.342	13.184

In order to shift the center frequency of the filter to a higher frequency, the total length of the resonator stages was reduced. Consequently, the length of all resonator stages was reduced to 12.5 mm from the calculated value of 13.1 mm to match the desired center frequency. On the other hand, the width of all resonator stages and the feed line were increased to 1.2 mm in order to increase the bandwidth of the filter. The spacing between the outer resonator stages ($S_{1,2}$ and $S_{4,5}$) were changed to 1.08 mm to achieve a better return loss whereas the inner stages' spacing was not modified.

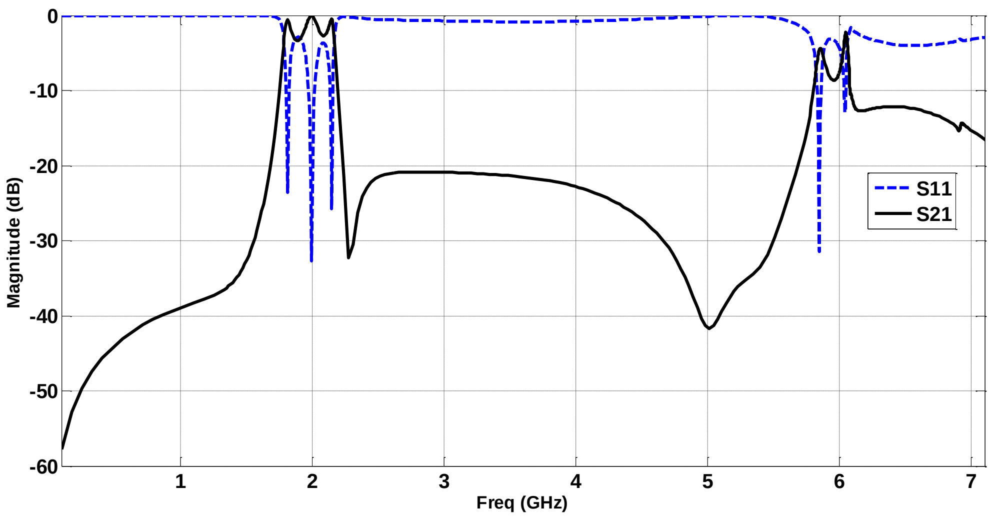


Figure 3.36: EM magnitude responses of the designed interdigital filter with $f_o = 2.05\ GHz$.

In order to further improve the S11 response (reflection coefficient), the position of the tapping line as well as the total length of the I/O resonator stages were optimized. Table 3.12 presents the final optimized dimensions of the interdigital filter to be fabricated for the LO channel of the radar system ($f_o = 2.05\ GHz, BW = 300\ MHz$).

Table 3.12: Final dimensions (in mm) of the optimized interdigital filter for LO channel (f_o= 2.05 GHz, BW= 300 MHz)

W_f	L_{tapp}	W_n	L_1, L_5	L_2, L_3, L_4	$S_{2,3}, S_{3,4}$	$S_{1,2}, S_{4,5}$
1.2	4	1.2	13.86	12.5	1.7	1.08

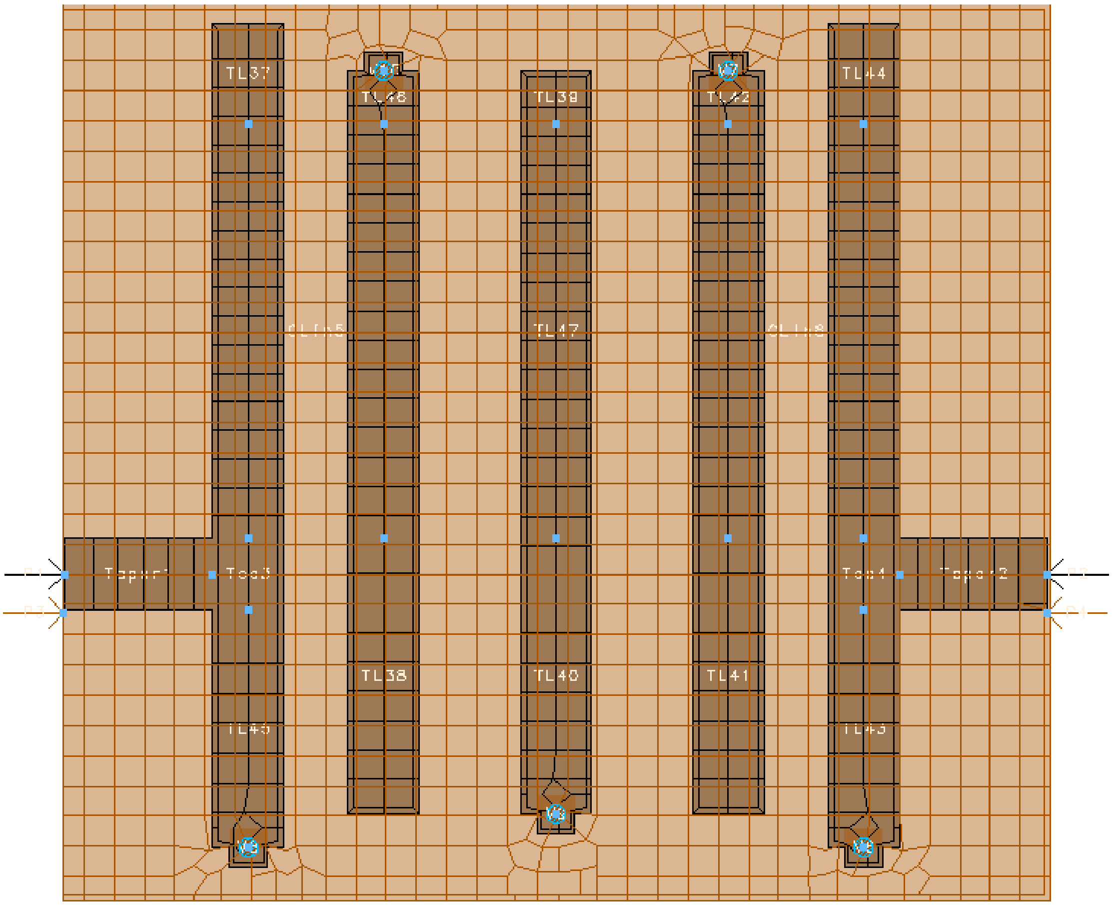
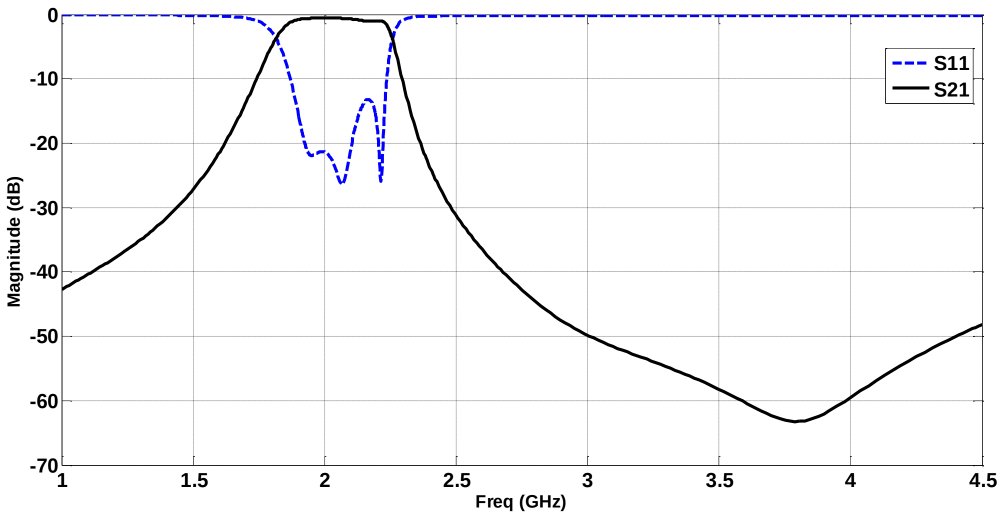
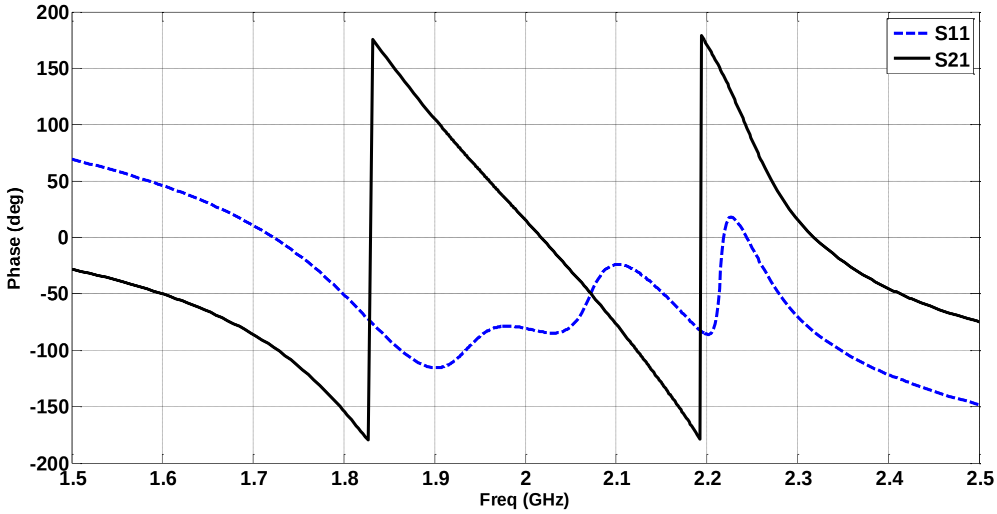


Figure 3.37: Layout of the optimized interdigital filter for LO channel (f_o = 2.05 GHz, BW = 300 MHz).

The layout of the final optimized interdigital filter for the LO channel is shown in Figure 3.37. The created mesh by the Momentum simulator is obvious and the 50 Ω ports determine the feed line position of the filter structure. The overall size of the filter is 16.6×15.1 mm^2. The EM simulation results of the filter are presented in Figure 3.38. As seen, the filter exhibits a low and flat insertion loss over the entire bandwidth and the return loss is optimal (better than -15 dB), indicating a low reflection over the pass band. The second harmonic of the pass band at 4.1 GHz is attenuated by more than -55 dB indicating a good rejection level for the upper side product of the mixer. Moreover, the phase response of the filter is linear indicating a constant group delay for all the desired frequencies.



(a)



(b)

Figure 3.38: EM simulation responses of the optimized final interdigital filter for LO channel (a) S11 and S21 magnitude (b) S11 and S21 phase.

3.10 Capacitively-Coupled BPF

The planar microstrip filters are not a suitable choice for low frequencies (< 1GHz) as the size of such filters become bulky. As discussed previously, the size of such distributed filters is proportional to the wavelength at the desired center frequency. The wavelength is inversely proportional to the frequency of operation.

The capacitively-coupled BPF is a well-known architecture for filters with narrow bandwidths (below 20%) which results in a realizable range of lumped element components. This type of BPF is promising for practical applications where the goal is to reduce the number of inductors as much as possible. The reason behind reducing the number of inductors in the design is the lack of availability of high quality factor (high-Q) inductors at high frequencies. The quality factor of the inductors is a measure of defining the inductance purity. It is defined as the ratio of the inductance over the resistance of the lumped inductor. In practical scenarios, lumped inductors are not ideal which introduce a resistive element into the circuits. The presence of a resistive element in a resonator circuit introduces losses in the circuit which consequently results in an increase in the insertion loss of the overall filter. In addition, the self-resonance of the lumped components at higher frequencies results in lowering the out-of-band rejections of the filter by creating spurious responses [81].

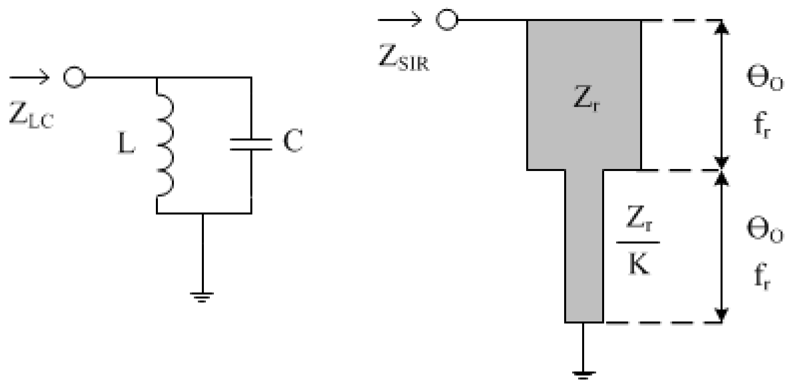
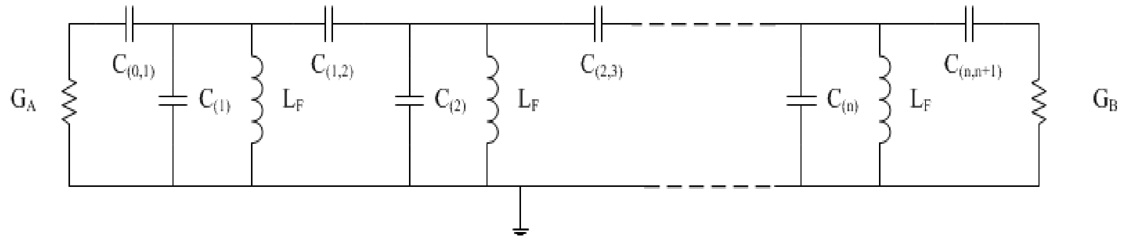


Figure 3.39: L-C resonator and its equivalent SIR.

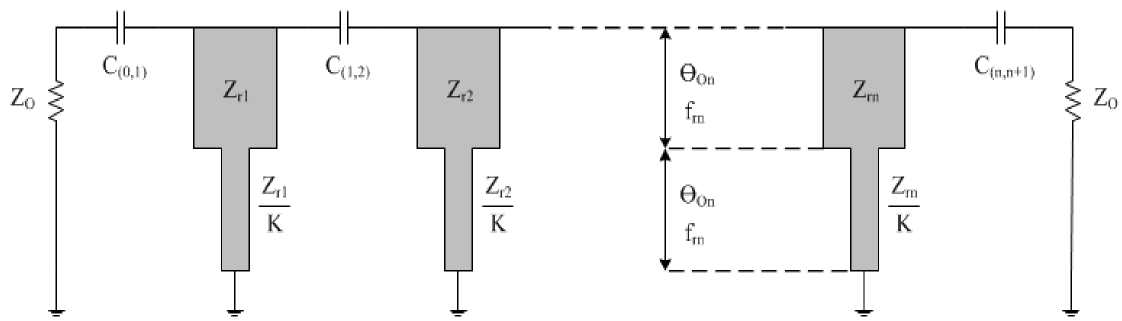
The capacitively-coupled (CC) BPF was selected to be used for the two different filters required for the RX channels of the radar system. For the first filter with a 760 MHz center frequency and 20 MHz bandwidth, a hybrid design of lumped components and distributed microstrip SIRs were utilized. The microstrip SIRs act as an L-C resonator providing the required resonance elements of the filter to avoid using low-Q lumped inductors at such frequencies. On the other hand, to achieve the required filtering for the second filter with a center frequency of 70 MHz and 16 MHz bandwidth, a pure lumped component BPF is a proper choice. The design of both BPFs starts with filter synthesis of the capacitively-coupled BPF. For the lumped-distributed filter, an extra step is required to transform the L-C resonators into their equivalent microstrip SIRs (Figure 3.39) for the desired filter's center frequency and bandwidth. The step-by-step design formulas of the capacitively-coupled BPFs for applications ranging from 500 MHz up to 1 GHz are presented in [82].

3.10.1 Capacitively-coupled BPF (750-770 MHz)

Figure 3.40 (a) depicts the schematic configurations of an n^{th} order capacitively-coupled BPF. As shown in the figure, the parallel resonators (L-C) in a pure lumped component capacitively-coupled BPF are coupled through the series capacitors which connect the two ports of the filter. The same filter structure can be implemented by transforming the L-C resonators into their equivalent distributed elements with the help of SIRs. The schematic of this filter structure is shown in Figure 3.40 (b).



(a)



(b)

Figure 3.40: n^{th} order CC BPF (a) Lumped *L-C* (b) Hybrid lumped-distributed

A fifth-order, 0.044 dB Chebyshev CC BPF was initially designed to verify the practicality of having a pure lumped element BPF at this frequency band. The center frequency of the filter is 760 MHz with a 5% fractional bandwidth, resulting in a pass band of 741-779 MHz. The inductor value was chosen to be 7 nH for the parallel resonators. The required capacitances for the resonators as well as the coupling capacitors were calculated using a developed MATLAB code.

Consequently, the calculated values of the components as well as the utilized practical lumped components (COTS) are presented in Table 3.13.

Table 3.13: Component values of the initially-designed CC BPF (f_o = 760 MHz,Δ = 0.05).

Component Ref	Calculated Value	Utilized off-the-shelf Value	Unit	Size
$C_{(0,1)}, C_{(5,6)}$	1.207	1.2	pF	0603
$C_{(1,2)}, C_{(4,5)}$	0.271	0.3	pF	0603
$C_{(2,3)}, C_{(3,4)}$	0.199	0.2	pF	0603
$C_{(1)}, C_{(5)}$	4.879	4.7	pF	0603
$C_{(2)}, C_{(4)}$	5.795	5.6	pF	0603
$C_{(3)}$	5.867	5.6	pF	0603
$L_{(n)}$	7	6.8	nH	2012

The schematic simulation of the filter was performed using the specified components in Table 3.13 and the S21 comparison results are plotted in Figure 3.41.

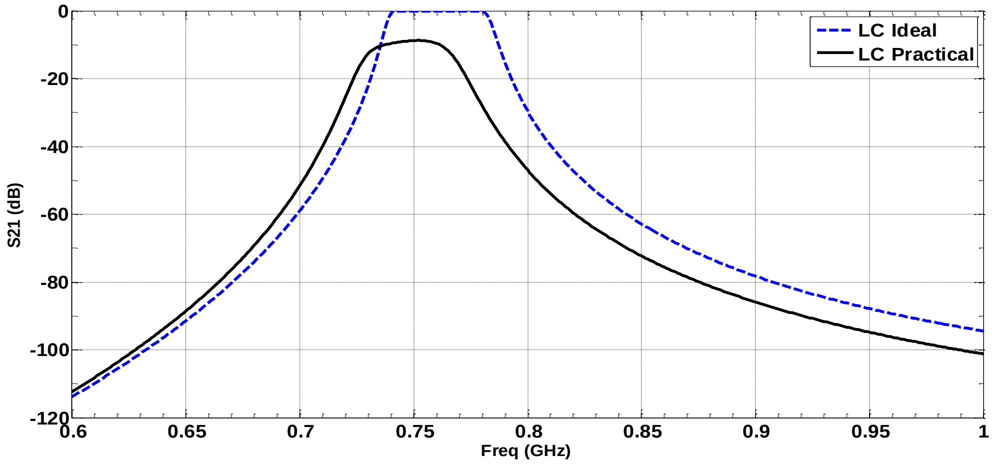


Figure 3.41: Ideal vs. practical responses of the initially designed CC BPF (f_o = 760 MHz).

As shown in the figure, the insertion loss of the filter is below -10 dB indicating a high loss in the filter. The center frequency of the filter is shifted to the left due to the difference in the exact values of the lumped components compared to the ideal ones. Nevertheless, the actual response of the filter will deteriorate further in reality as the board's parasitics are not considered in this simulation.

The equivalent SIRs for the parallel L-C resonator circuits were calculated. A value of 0.5 was chosen for the SIR impedance ration (K) which results in an equivalent electrical length of $\theta = 35.2°$. After obtaining the characteristic impedances of the SIRs and their resonance frequencies, the values were inserted into LineCalc. Consequently, the width (W) and length (L) of the equivalent microstrip lines with an electrical length of 35.2° for the Rogers 6010 substrate and 1.27 mm thickness were obtained. The characteristic impedances and resonance frequencies of different resonator stages along with their dimensions are presented in Table 3.14. As is shown in the table, the widths of the lower microstrip lines are smaller due to the increase in their impedances as the K ratio was chosen to be less than 1.

Table 3.14: Different parameters of resonator stages for initially designed CC BPF ($K = 0.5$) for Rogers 6010 substrate.

n	Upper Microstrip			Lower Microstrip			$f_r(MHz)$
	$Z_r(\Omega)$	$W_n(mm)$	$L_n(mm)$	$Z_r/K\,(\Omega)$	$W_{nn}(mm)$	$L_{nn}(mm)$	
1	22.612	4.412	12.200	45.223	1.413	13.036	861.181
2	21.168	4.835	13.227	42.335	1.607	14.116	790.215
3	21.071	4.865	13.304	42.143	1.621	14.197	785.363
4	21.168	4.835	13.227	42.335	1.607	14.116	790.215
5	22.612	4.412	12.200	45.223	1.413	13.036	861.181

Co-simulation of ADS is used for such circuit configurations where microstrip structures along with lumped components are used. In such simulations, the full-wave EM Momentum simulator is used to simulate the planar structures, their coupling, and layout parasitic effects. Consequently, the ADS circuit simulator is used to simulate the effects of the lumped components. Figure 3.42 represents the developed co-simulation in ADS where T-lines are used to connect the microstrip resonators to the capacitors' pads and via models are used for grounding purposes. It is noted that the resonator stages are placed in anti-directions in order to minimize the effects of mutual coupling between different stages. The width of the feed lines at 760 MHz was calculated to be 1.148 mm in order to have a 50 Ω microstrip line.

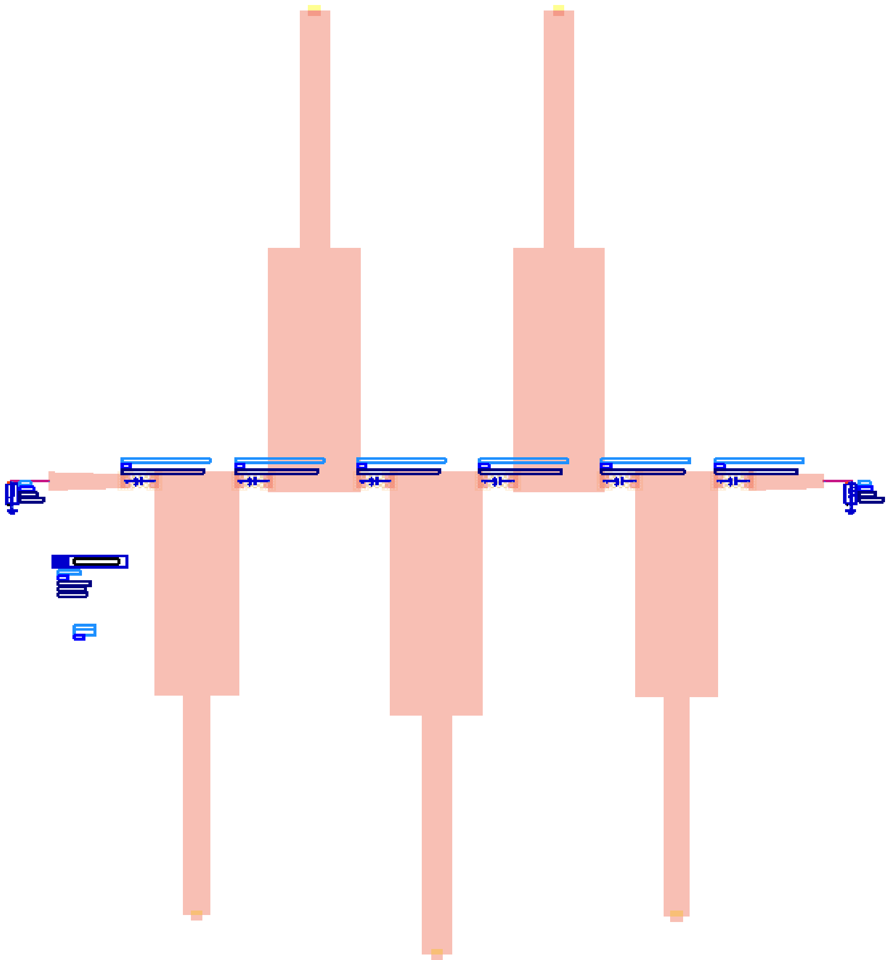
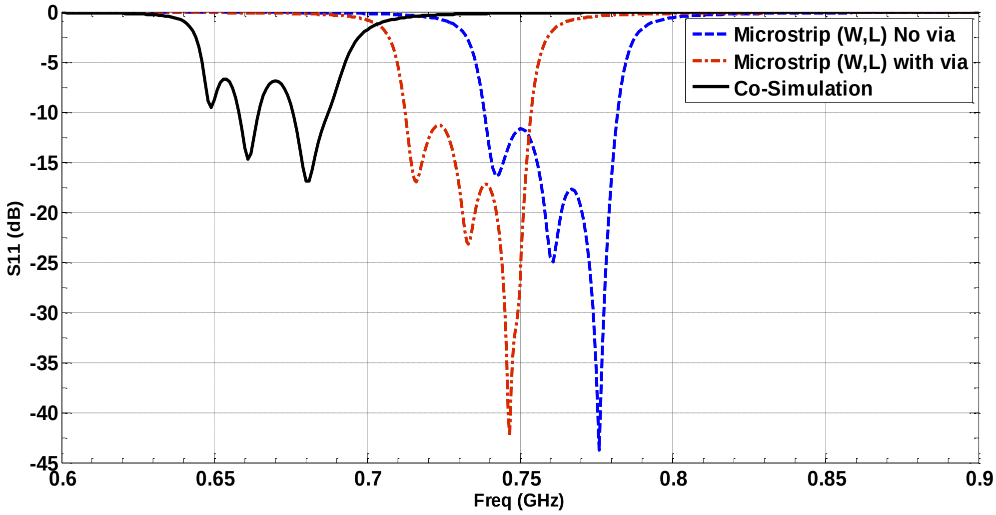
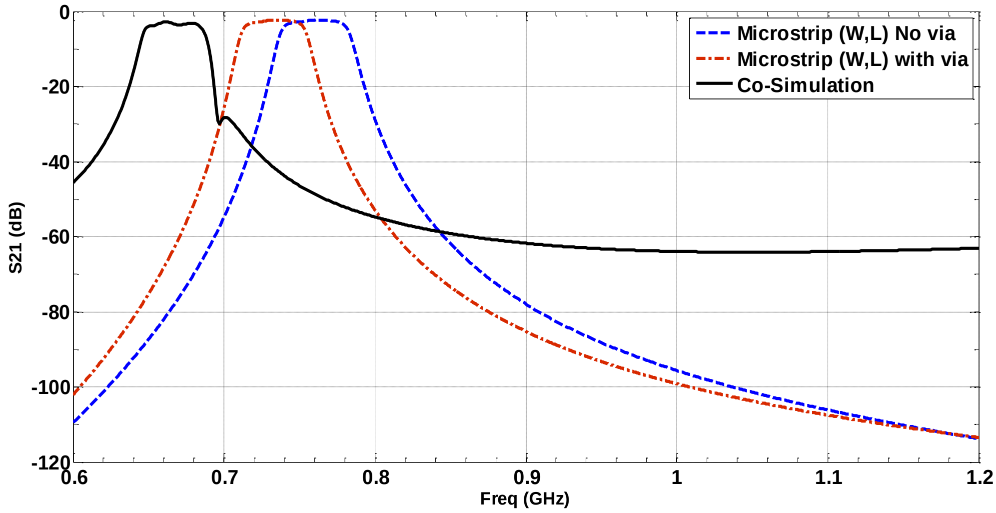


Figure 3.42: Capacitively-coupled BPF (a) Schematic (b) Co-simulation.

The comparison of the designed BPF with different simulation types is presented in Figure 3.43. In addition to the co-simulation, the circuit simulation was performed with and without including the grounding via models. The responses of the filter for different simulation types are approximately similar with the same bandwidth and a shift in the center frequency. It is observed that the desired filter response and the center frequency are achieved for the circuit simulation when the grounding vias are not included. However, the added grounding vias act as added inductors at high frequencies which are in series with the parallel L-C resonators and affect the resonance frequency of each stage. This causes a shift in the center frequency of the filter. Hence, co-simulation is the best solution in order to appropriately model the introduced vias at the operating frequencies.



(a)



(b)

Figure 3.43: Comparison between the circuit simulation and co-simulation of CC BPF.

The center frequency of the filter in the circuit simulation without including the ground vias is 760 MHz with a pass band of 741-779 MHz, similar to the designated values. The center frequency of the filter in the circuit simulation with the vias included is 732 MHz with a pass band of 713-751 MHz. The center frequency of the filter in the co-simulation is shifted to 667 MHz with a pass band of 649-685 MHz. From these results, it is concluded that the bandwidth of the filter is similar to the designated value of 38 MHz, independent of simulation type. Moreover, the insertion loss of the filter is approximately similar in all cases as well. However, the return loss is degraded in the co-simulation as a result of improper impedance matching.

3.10.1.1 Shift in the center frequency by varying the resonators' lengths

The center frequency of a planar structure is inversely proportional to its resonators' lengths. As the lengths of the resonators get longer, the center frequency of the hybrid capacitively-coupled BPF decreases. From the previous co-simulation results shown in Figure 3.43, the center frequency of the designed structure is shifted to a lower frequency of 667 MHz. Hence, the lengths of the resonators should be decreased in order to shift the center frequency of the filter towards the higher frequencies (the desired 760 MHz).

As a first trial, the length of each microstrip line of SIR stages was rounded to the closest integer value and then reduced by 2 mm, causing a 4 mm reduction in the total SIRs' lengths. Hence, co-simulation of the schematic and layout was performed and the overall response of the filter was obtained. From the results, it was found that the center frequency was shifted to 775 MHz, which is higher than the desired value of 760 MHz. The pass band of the filter was found to be 747-803 MHz. Hence, the length of all resonators should be increased to shift the filter's response down to lower frequencies.

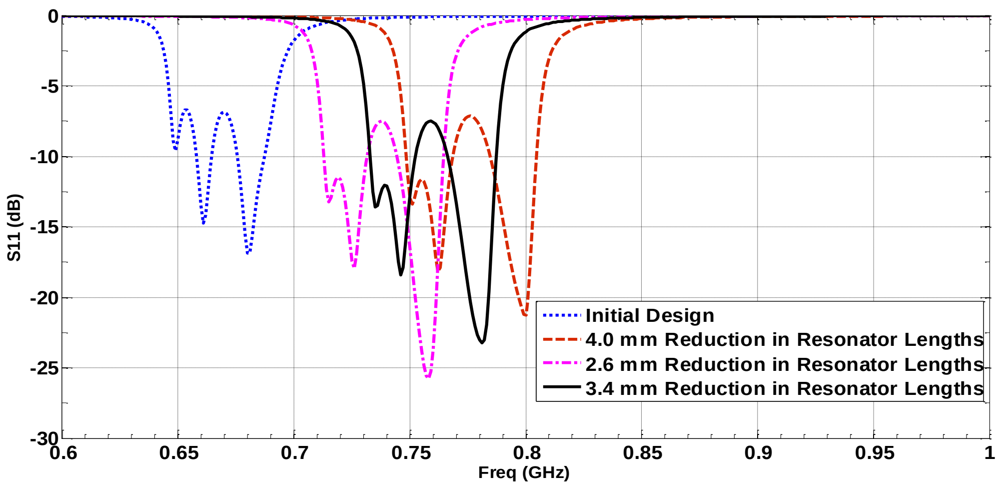
As a second trial, the length of each microstrip section of SIRs was increased by 0.7 mm, causing a total decrease of 2.6 mm in the lengths of the SIRs with respect to the original design. The center frequency of the filter after co-simulation was found to be 737 MHz with a pass band of 711-763 MHz. As a comparison with the initial trial, the center frequency of the filter is shifted down to a lower frequency with the increase in the total lengths of the SIRs. The bandwidth of the filter is approximately unchanged compared to the previous case. Hence, the total lengths of the SIRs should be decreased slightly to obtain the desired center frequency of 760 MHz.

As the last optimization, the length of each microstrip line was decreased by 0.4 mm with respect to the second trial. This resulted in a decrease of 3.4 mm in the total lengths of the resonators compared to the initial design. The lengths of SIRs in different optimization trials are summarized in Table 3.15 and the co-simulation comparison results are presented in Figure 3.44. As is seen, the center frequency of the filter is at 760 MHz with a bandwidth of 731-786 MHz. Compared to the required bandwidth of 20 MHz for the filter, the wider bandwidth is desired due to the probabilistic reduction in the bandwidth of the fabricated filter due to the fabrication and lumped capacitance tolerances.

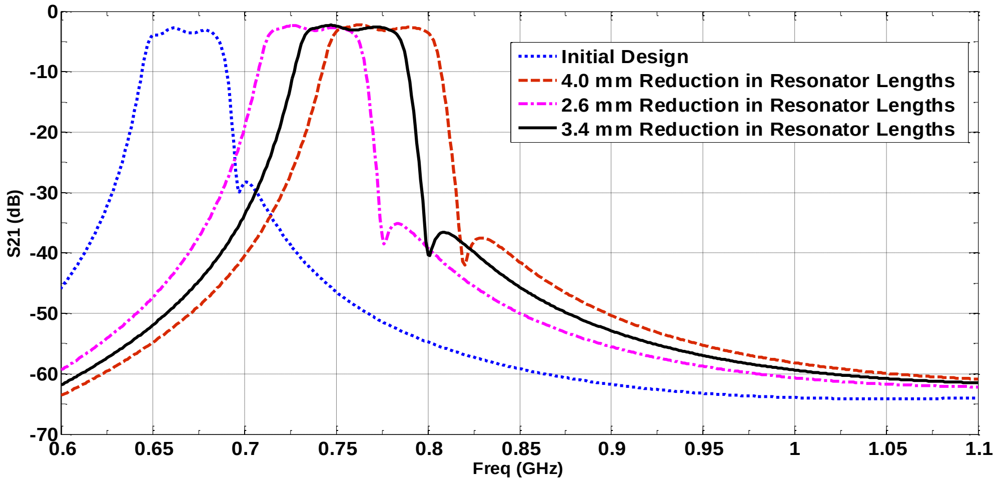
It is obvious from Figure 3.44 that the return loss of the filter in all cases follows the same pattern and is above -10 dB, indicating a high reflection over the pass band of the filter. Hence, the next optimization task is to enhance the reflection coefficient of the filter by improving the impedance matching of the filter and the source impedance.

Table 3.15: Lengths of SIRs for each optimization trial.

n	Original		First Trial (4.0 mm reduction)		Second Trial (2.6 mm reduction)		Third Trial (3.4 mm reduction)	
	$L_n(mm)$	$L_{nn}(mm)$	$L_n(mm)$	$L_{nn}(mm)$	$L_n(mm)$	$L_{nn}(mm)$	$L_n(mm)$	$L_{nn}(mm)$
1	12.200	13.036	10	11	10.7	11.7	10.3	11.3
2	13.227	14.116	11	12	11.7	12.7	11.3	12.3
3	13.304	14.197	11	12	11.7	12.7	11.3	12.3
4	13.227	14.116	11	12	11.7	12.7	11.3	12.3
5	12.200	13.036	10	11	10.7	11.7	10.3	11.3



(a)



(b)

Figure 3.44: Effect of SIR lengths on the response of CC BPF.

3.10.1.2 Return loss improvement of the optimized BPF

In all previous cases, the values of the coupling capacitors between all resonator stages were as follows: $C_{(0,1)} = C_{(5,6)} =$ 1.2 pF, $C_{(1,2)} = C_{(4,5)} =$ 0.3 pF, and $C_{(2,3)} = C_{(3,4)} =$ 0.2 pF. It was found that different combinations of the available COTS capacitors could be used in order to improve the return loss response of the optimized BPF. Table 3.16 lists the final SIR dimensions of the BPF along with the required lumped capacitors for the coupling stages. All the lumped capacitors of the design are chosen to be with a package size of 0603. The final dimension of the filter's layout is 40.7 × 49 mm^2.

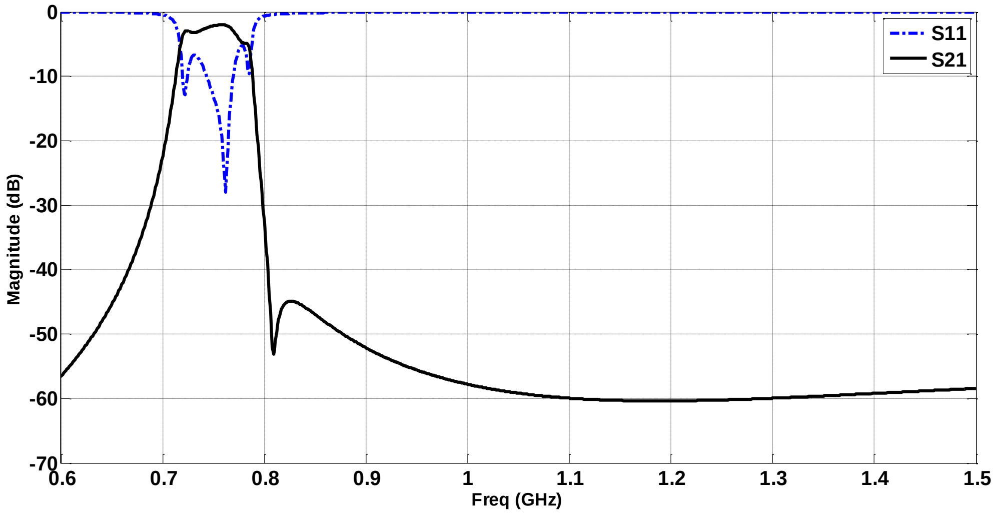
Table 3.16: Final optimized SIR dimensions and capacitor values for CC BPF (f_o = 760 MHz).

n	Upper Microstrip		Lower Microstrip	
	$W_n(mm)$	$L_n(mm)$	$W_{nn}(mm)$	$L_{nn}(mm)$
1	4.41	10.3	1.41	11.3
2	4.83	11.3	1.61	12.3
3	4.87	11.3	1.62	12.3
4	4.83	11.3	1.61	12.3
5	4.41	10.3	1.41	11.3

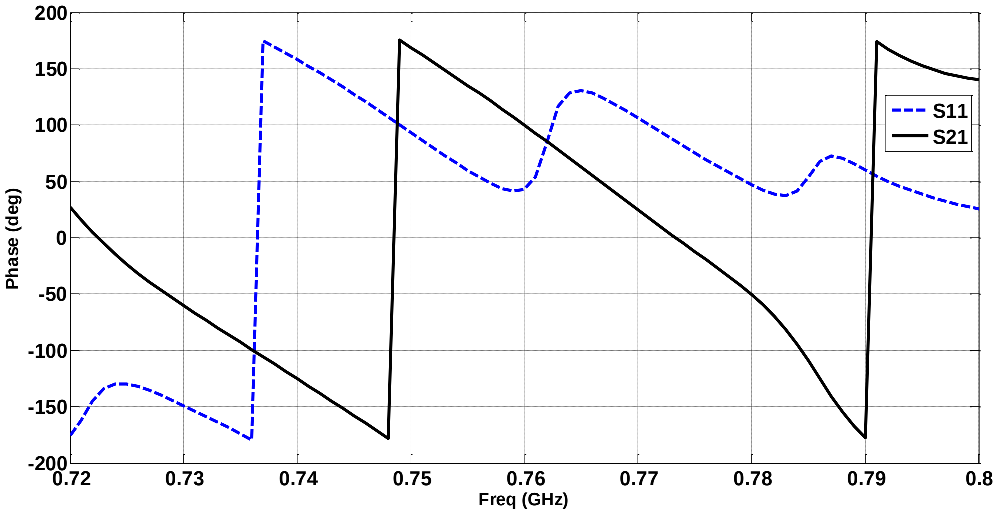
Cap.	pF
$C_{(0,1)}$	1.5
$C_{(1,2)}$	0.3
$C_{(2,3)}$	0.3
$C_{(3,4)}$	0.3
$C_{(4,5)}$	0.3
$C_{(5,6)}$	1.5

Figure 3.45 depicts the S11 and S21 magnitude and phase responses of the final optimized capacitively-coupled BPF. The insertion loss of the filter is low within

the bandwidth which is centered at 760 MHz. The return loss response of the filter over the pass band is well below the standard -10 dB, indicating a good impedance matching of the filter with the 50 Ω. The phase response of the filter is also linear over the pass band, indicating the desirable constant delay of the signals at the desired frequencies which avoid signal dispersion.



(a)



(b)

Figure 3.45: Co-simulation response of the final optimized hybrid CC BPF for the RX channels (f_o = 760 MHz).

3.10.2 Capacitively-Coupled BPF (62-78 MHz)

With the design of the hybrid capacitively-coupled BPF with a center frequency of 760 MHz, the design of the pure lumped components L-C BPF is easy and straightforward. In this section, the design of a CC lumped L-C component filter with a center frequency of 70 MHz and 16 MHz bandwidth (62-78 MHz) is discussed. The filter is intended to be used as the last filter in the RX channels of the radar system. The operating frequency of the filter is low, making the lumped components the best solution for its implementation. At such frequencies, off-the-shelf lumped inductors with reasonable quality factors are commercially available. Choosing the best inductor with a high Q-factor at the operating frequency is critical in reducing the overall insertion loss of the filter.

After designing several filters, a recurring 4 MHz shift in the center frequency was observed in all designs. Hence, the filter was redesigned for a center frequency of 66 MHz in order to account for the 4 MHz frequency shift. This resulted in a filter with a center frequency of 70 MHz. The bandwidth of the filter was chosen to be 55-76 MHz. The inductor value of 100 nH was selected for the resonator stages. Table 3.17 lists the calculated versus the used off-the-shelf components of the designed BPF.

Table 3.17: Component values for the designed lumped CC BPF.

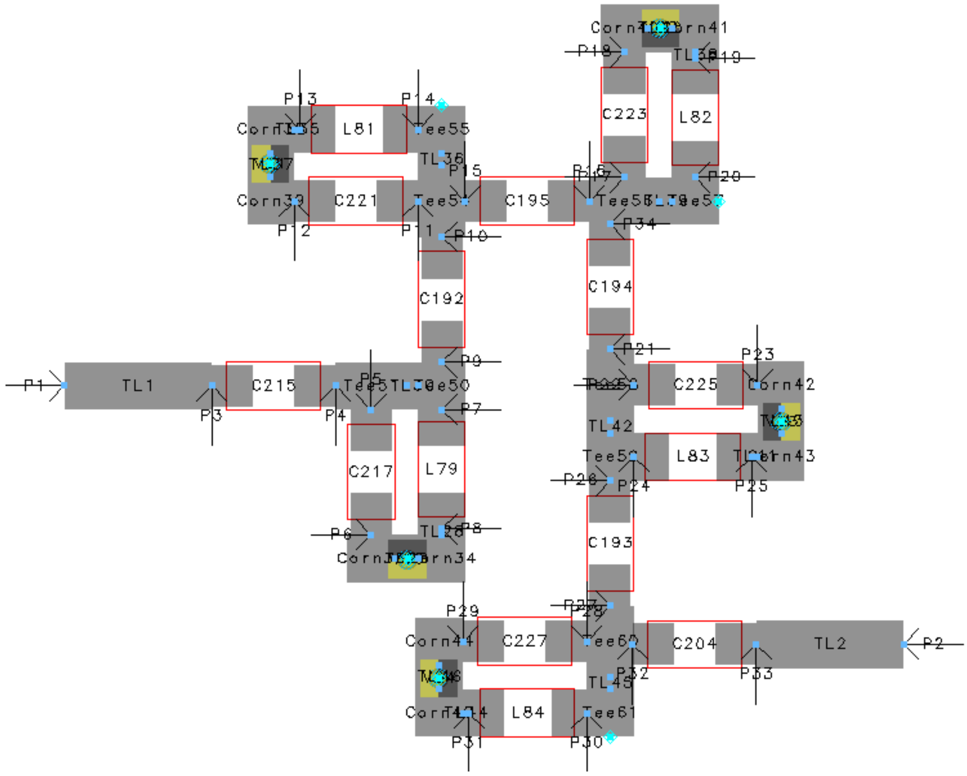
Component Ref	Calculated Value	Utilized off-the-shelf Value	Unit	Size
$C_{(0,1)}, C_{(5,6)}$	38.855	39	pF	110
$C_{(1,2)}, C_{(4,5)}$	16	16	pF	110
$C_{(2,3)}, C_{(3,4)}$	11.757	12	pF	110
$C_{(1)}, C_{(5)}$	18.589	18	pF	110
$C_{(2)}, C_{(4)}$	30.393	30	pF	110
$C_{(3)}$	34.636	33	pF	110
$L_{(n)}$	100	100	nH	1608 (0603)

In addition to the ideal and practical schematic simulations, the co-simulation was also performed for the developed layout of the filter. Figure 3.46 (a) shows the created layout for the BPF using lumped components. The pads of all lumped components were placed in the layout and these components were connected by very short microstrip lines. The layout of the filter is very compact, occupying an overall area of $14.3 \times 12.4\,\mathrm{mm}^2$. The lumped inductors of different resonator stages are positioned at 90° with respect to each other to avoid possible mutual coupling between them which would affect the overall response of the filter. The ports added to the layout of the filter determine the locations at which the lumped components are to be connected when performing co-simulation in ADS. Figure 3.46 (b) depicts the co-simulation setup of the filter in ADS with the EM model and the added lumped components.

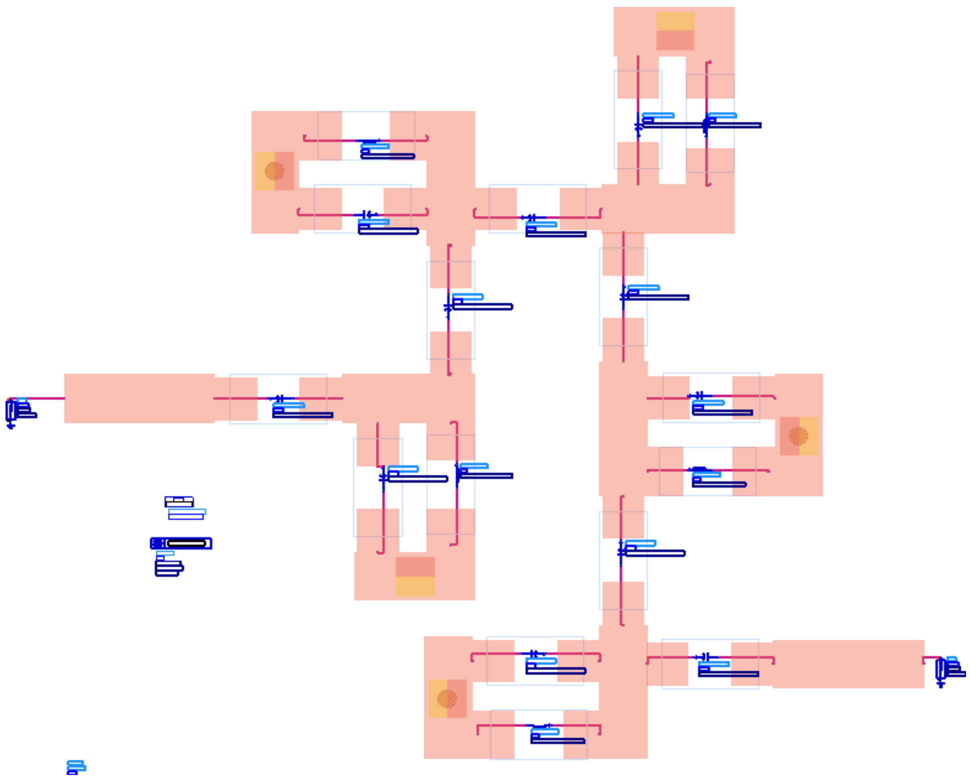
The results of the schematic and co-simulation for the developed BPF using off-the-shelf lumped components along with the ideal schematic responses are shown in Figure 3.47. As it is seen, the insertion loss of the filter is deteriorated compared to the ideal case. However, this is the best achievable response using the practical lumped components. In addition, the return loss of the filter is well below the standard -10 dB, indicating minimal reflections over the filter's pass band. The rejection and reflection responses of the filter are approximately similar for different simulations due to their low operating frequency. At these frequencies, the vias do not affect the resonator stages, unlike the previously designed BPF at 760 MHz. Similar results of the schematic simulation using practical components and its co-simulation indicate minimal parasitic effects of the created layout at the operating frequencies.

Although the developed L-C BPF exhibits the desired insertion and return loss responses, the used capacitors were not commercially available at the distributor center when ordering components. Hence, the design capacitors were replaced and optimized with the available capacitors by the distributor. Table 3.18 presents the final values of the utilized lumped components in the design of the L-C BPF.

The schematic and co-simulation comparison results of the final designed lumped element BPF using the presented components in Table 3.18 are presented in Figure 3.48. As it is seen from the plots, the return loss of the filter over the pass band is well below -25 dB which indicates good impedance matching between the filter and the 50 Ω characteristic impedance of the system. In addition, the filter exhibits an acceptable insertion loss as well as rejection behavior at the desired frequencies. The bandwidth of the filter is higher than the desired value due to the possible decrease in the bandwidth or possible shift in the center frequency of the fabricated filter (due to the tolerances in the fabrication and the exact components' values). The phase response of the filter is linear over the pass band which is desired to avoid signal dispersion at the desired frequencies.

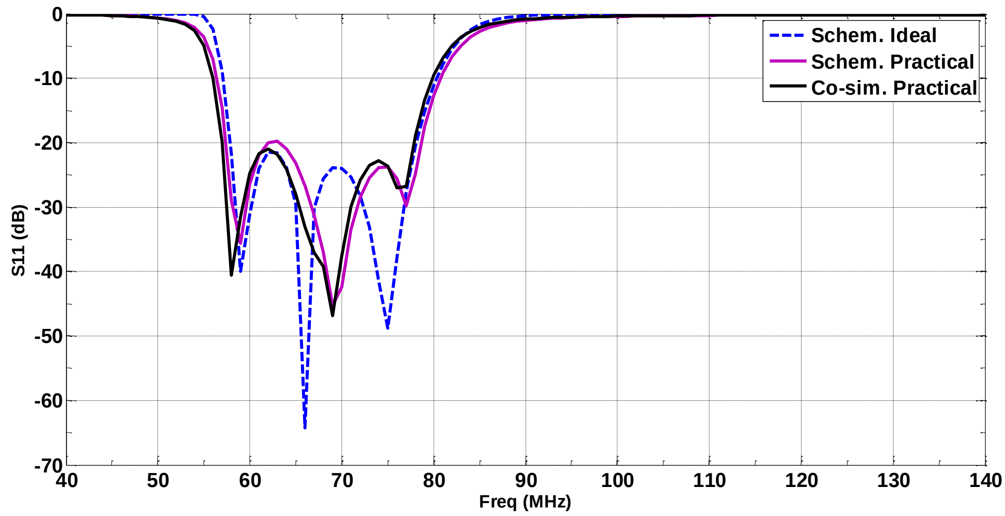


(a)

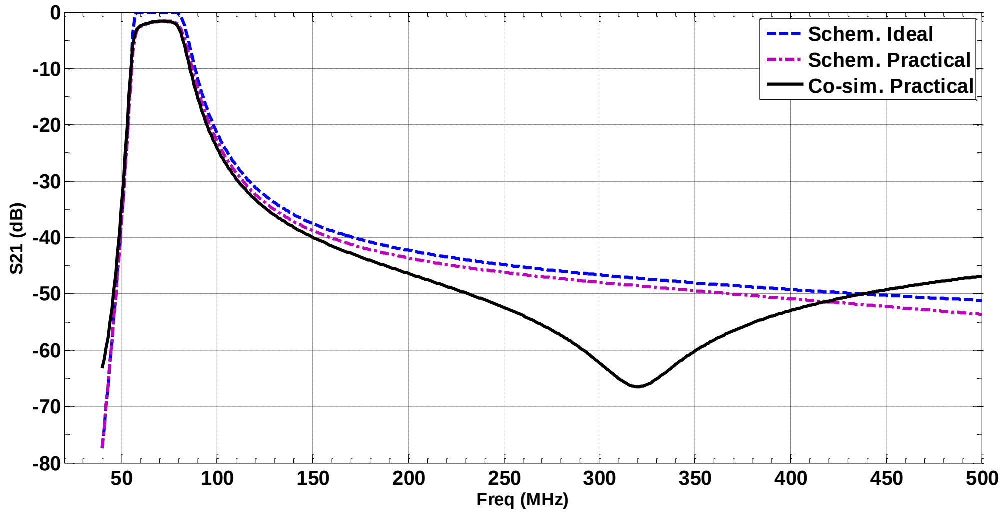


(b)

Figure 3.46: Developed CC L-C BPF (f_o = 70 MHz) (a) Layout (b) Co-simulation.



(a)

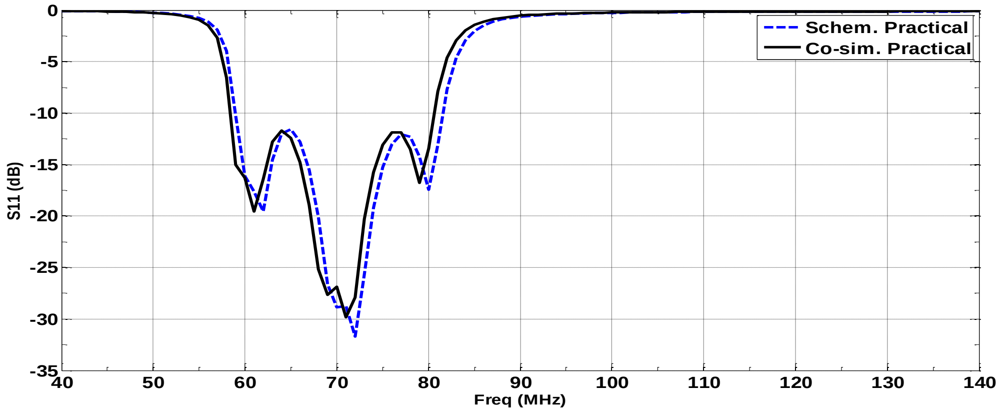


(b)

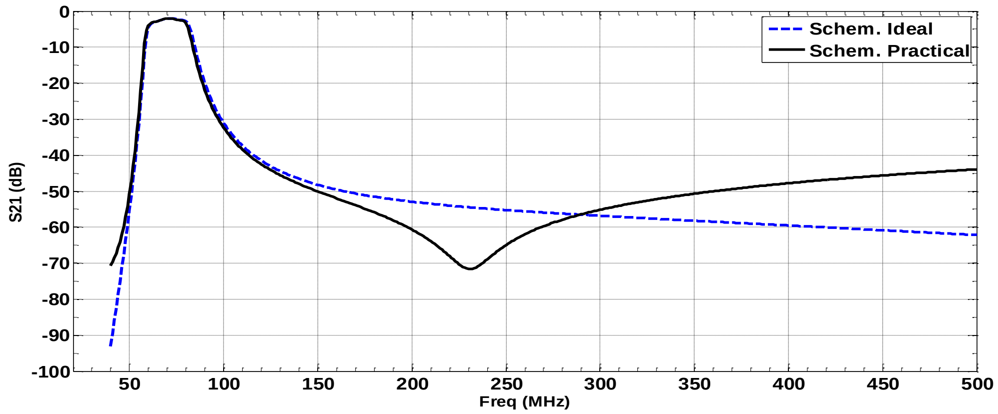
Figure 3.47: Ideal vs. practical and co-simulation responses of the developed CC BPF (f_o = 70 MHz).

Table 3.18: Final component values to be soldered on PCB for the designed lumped CC BPF (f_o = 70 MHz).

Component Ref	**Calculated Value**	**Utilized off-the-shelf Value**	**Unit**	**Size**
$C_{(0,1)}, C_{(5,6)}$	38.855	27	pF	1608 (0603)
$C_{(1,2)}, C_{(4,5)}$	16	12	pF	1608 (0603)
$C_{(2,3)}, C_{(3,4)}$	11.757	10	pF	1608 (0603)
$C_{(1)}, C_{(5)}$	18.589	22	pF	1608 (0603)
$C_{(2)}, C_{(4)}$	30.393	33	pF	1608 (0603)
$C_{(3)}$	34.636	33	pF	1608 (0603)
$L_{(n)}$	100	100	nH	1608 (0603)



(a)



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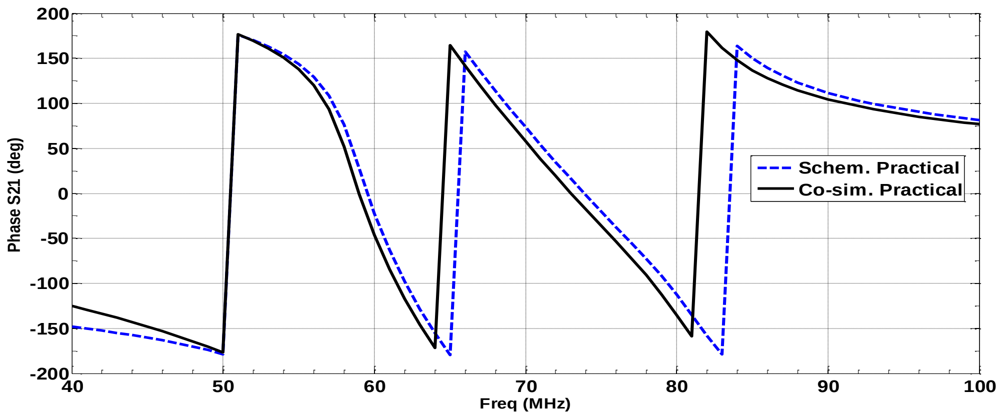


(c)

Figure 3.48: Response of the final developed lumped element CC BPF (f_o = 70 MHz) (a) S11 magnitude (b) S21 magnitude (c) S21 phase.

Chapter 4: PCB Development and Design of Radar Testbed

The overall radar system was integrated on PCB using the aforementioned designed filters in Chapter 3. A crucial factor in the system design was matching the impedance levels of individual blocks to the system's characteristic impedance in order to achieve maximum power transfer. The 50 Ω standard characteristic impedance was selected for the system and the impedance of each block was matched to that value at the desired frequency bands. As discussed in the previous chapter, all filters were optimized for the 50 Ω impedance, and hence were easily integrated into the system without any need for further modification. This chapter discusses the simulation and optimization of the utilized ICs in the radar testbed, in addition to the PCB integration for the TX-LO and RX channels.

4.1 Amplifiers Impedance Matching

As discussed in Chapter 2, two different amplifiers, Analog Devices ADL5602 and Avago Technologies MGA30789, were used for the TX-LO channels whereas the SBB1089Z of RFMD was used for all the required amplification stages of the RX channels. These amplifiers were selected since they were internally matched to 50 Ω over their specified operating range of frequencies. However, the impedance matching at all frequencies was not up to standard and external impedance matching was essential at the frequencies of interest. Hence, stepped-impedance matching was found to be an appropriate method as improvement was seen in the return loss responses of the amplifier circuits. This was achieved by changing the width of the microstrip transmission lines at the I/O ports of the amplifiers. This method was simply implemented using the micostrip technology without adding any extra cost to the overall system fabrication and without the need for any external lumped components.

The simulation was performed by adding the solder PADs for each amplifier and the external passive components (capacitors and inductors) in the layout. Consequently, the schematic-layout co-simulation was performed for each amplifier circuit. The S-parameters of the amplifiers were provided by the manufacturers in S2P format (Touchstone file for two port network). The behavioral models of the utilized lumped components were also provided by the manufacturers. These manufacturer-provided properties were then imported into ADS for the precise modeling of the amplifier circuits. The co-simulation of each amplifier circuit is presented in the following sections.

4.1.1 First-Stage Amplifiers for TX-LO Channels (ADL5602)

The first stage amplifier is the ADL5602 which is an RF gain block with an approximate gain of 19 dB in the SOT-89 package. For the radar testbed, this amplifier is to be operated from 1.52-1.82 GHz for the TX channel and 1.9-2.2 GHz for the LO channel. Figure 4.1 below shows the application circuit of this RF amplifier provided in its datasheet [83].

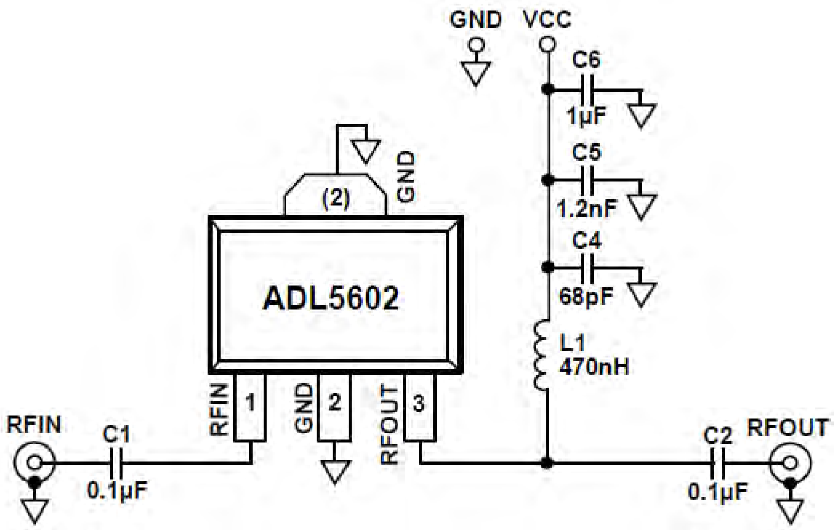


Figure 4.1: Application circuit of ADL5602 [83].

In the above figure, C_1 and C_2 represent the input and output AC-coupled capacitors required for the input and output RF signals, respectively. The DC biasing (+5 Volts) of the amplifier is supplied through the 470 nH bias inductor (L_1) to the output RF port and the power supply is decoupled using (C_4, C_5, and C_6) to reject the power supply noise. The amplifier consumes 89 mA of DC current under typical conditions. Table 4.1 lists the utilized surface mount lumped components for ADL5602 to be used in the TX and LO channels of the radar's PCB.

Table 4.1: Utilized lumped components for ADL5602 amplifier.

Component Ref	Datasheet Requirement	Utilized off-the-shelf Value	Unit	Size
C_1	0.1	0.1	µF	2012 (0805)
C_2	0.1	0.1	µF	2012 (0805)
C_4	68	68	pF	1005 (0402)
C_5	1.2	1.2	nF	2012 (0805)
C_6	1	1	µF	2012 (0805)
L_1	470	470	nH	1608 (0603)

Although the gain (S21) is fair enough as was taken into account in the frequency plan of the system, the return loss (S11) of ADL5602 is not below -10 dB for our frequency band of interest. This results in partial reflection of the signal at the input of the amplifier and reduces the signal's power. Hence, a proper impedance matching was required to improve the overall response of the amplifier at desired frequencies.

Figure 4.2 shows the ADS co-simulation of ADL5602 for the TX and LO channels. The layouts of the circuits were created and the EM model of the layout was inserted into the schematic to perform the co-simulation. As it is seen, the stepped-impedance was achieved by having two different widths of 2 mm (for length of 7 mm) and 1 mm in the input and output microstrip transmission lines to enhance the input and output reflections (return loss) of the amplifiers. While straight transmission lines with 90° bending were found to be better for ADL5602 in the TX channel, curved lines were used to improve the overall response of ADL5602 in the LO channel. The green box indicates the package area of the amplifier where the amplifier is to be soldered and the copper area (in black) beneath it shows the created PAD for the amplifier along with the grounding via holes. Several vias were used to provide the grounding path for the amplifier and to minimize the thermal impedance for heat dissipation. The blue components represent the models of different components in the co-simulation.

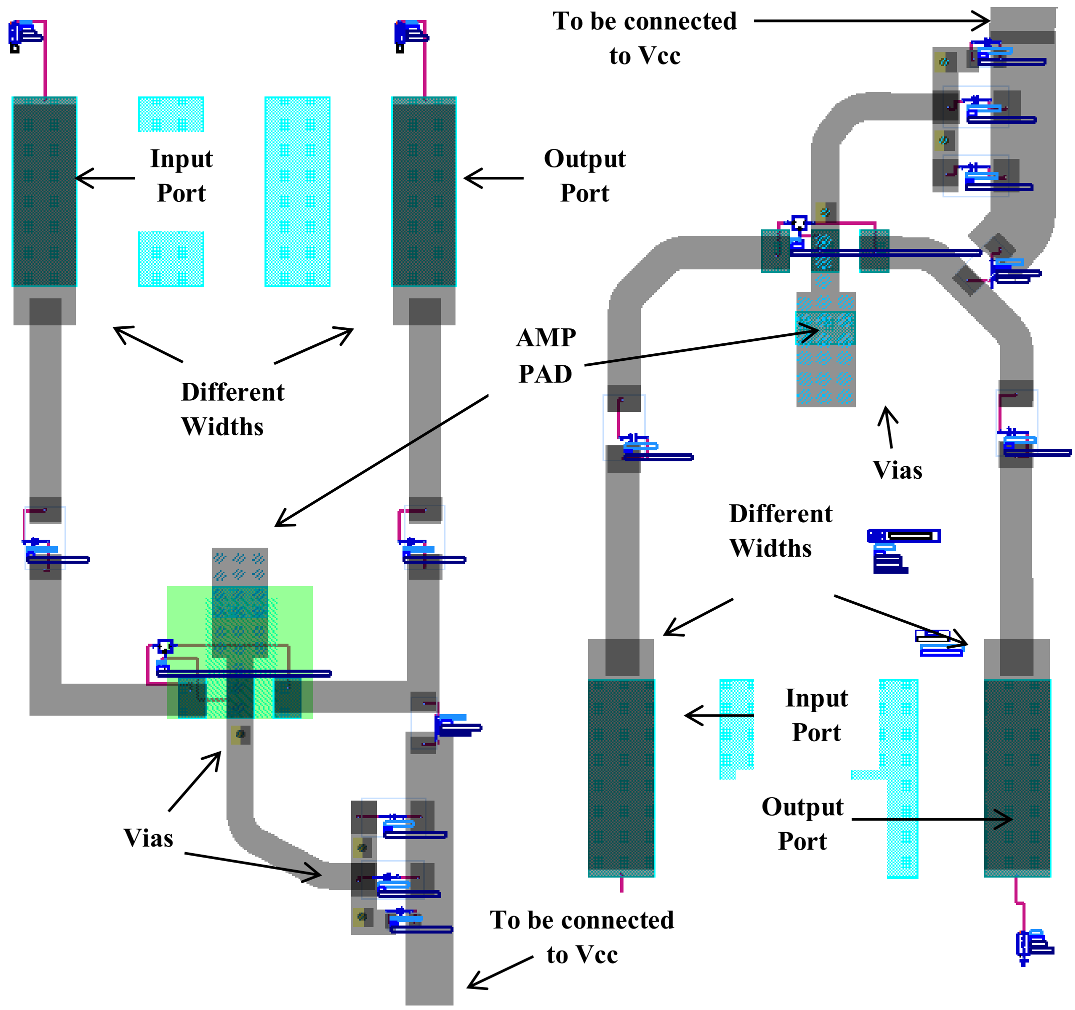
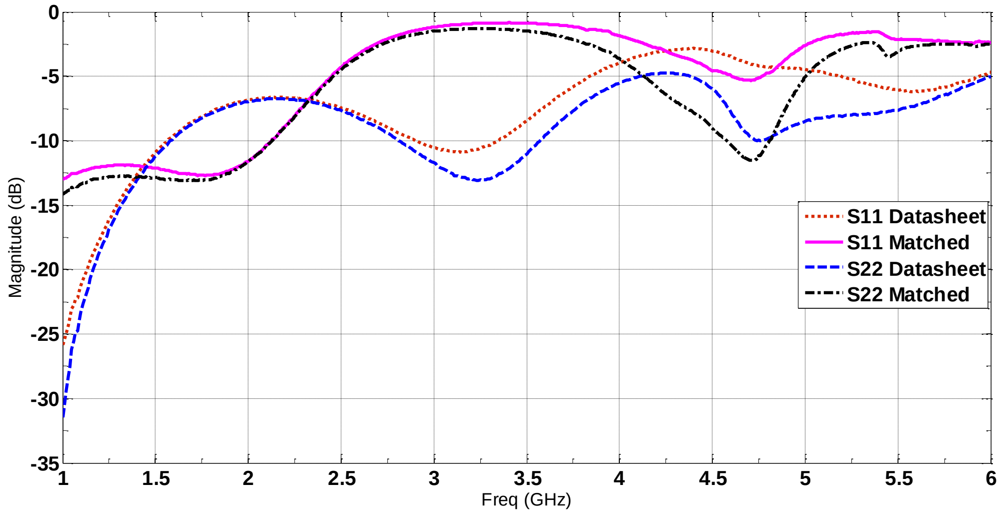
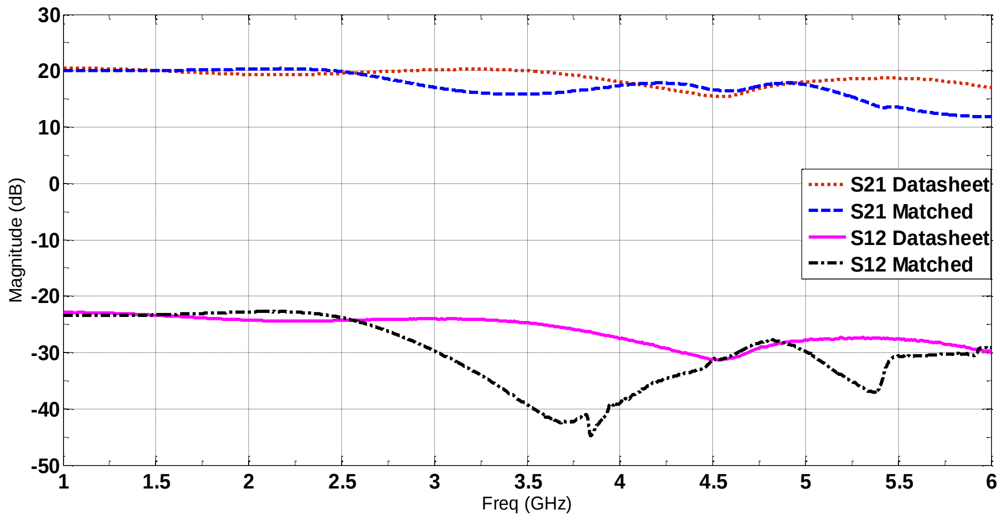


Figure 4.2: ADS co-simulation of ADL5602. TX channel Q1 (Left), LO channel Q3 (Right).

Figure 4.3 and Figure 4.4 represent a comparison between the datasheet responses of ADL5602 provided by the manufacturer along with the optimized matched responses for the TX and LO channels, respectively. From the S11 plots, it is clear that the datasheet's input and output return losses of ADL5602 are above -10 dB in the desired frequency ranges (1.52-2.2 GHz). However, the input and output return losses are improved to be better than -10 dB at the desired frequency bands of 1.52-1.82 GHz and 1.9-2.2 GHz for the TX and LO channels, respectively. Furthermore, the flatness of the gain (S21) and the reverse isolation (S12) patterns of the amplifiers are not affected in the frequency bands of interest.

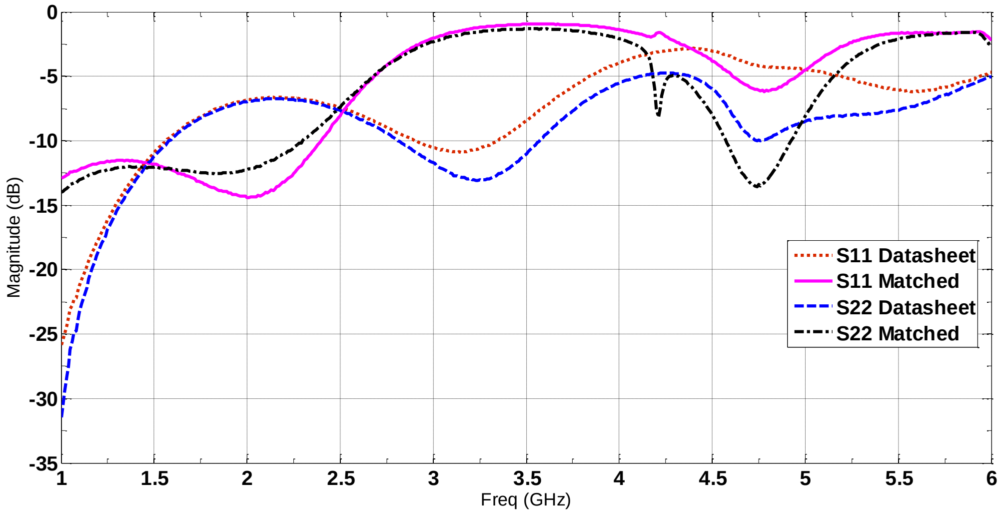


(a)



(b)

Figure 4.3: Datasheet vs. matched co-simulation S-parameter responses of ADL5602 for TX channel.



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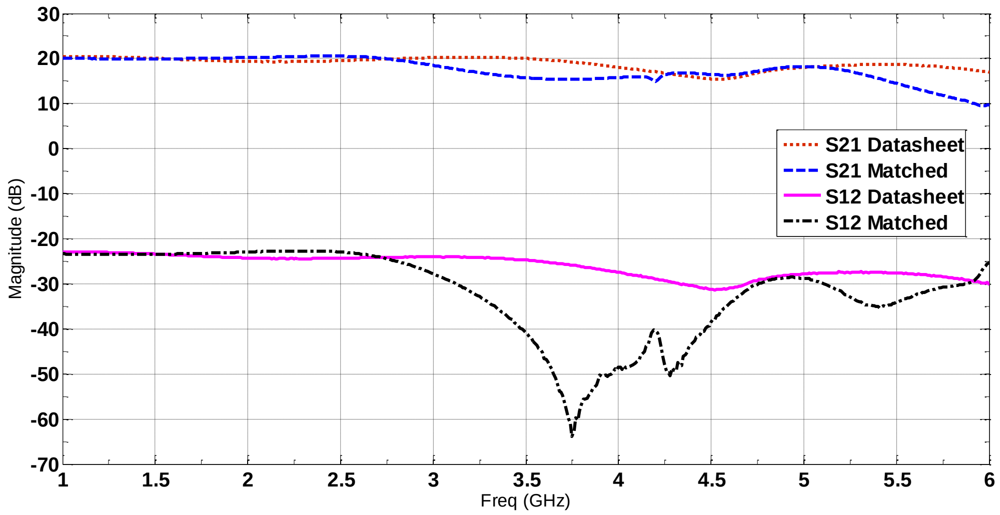


(b)

Figure 4.4: Datasheet vs. matched co-simulation S-parameter responses of ADL5602 for LO channel.

4.1.2 Second-Stage Amplifiers for TX-LO Channels (MGA30789)

The second stage amplifiers in the TX-LO channels are Avago Technologies' MGA30789 amplifier due to its high reported linearity. The amplifier is available in the SOT-89 package. For the radar testbed, this amplifier is to be operated from 3.04-3.64 GHz for the TX channel and 3.8-4.4 GHz for the LO channel. Figure 4.5 shows the general application circuit of MGA30789 provided in the datasheet [84].

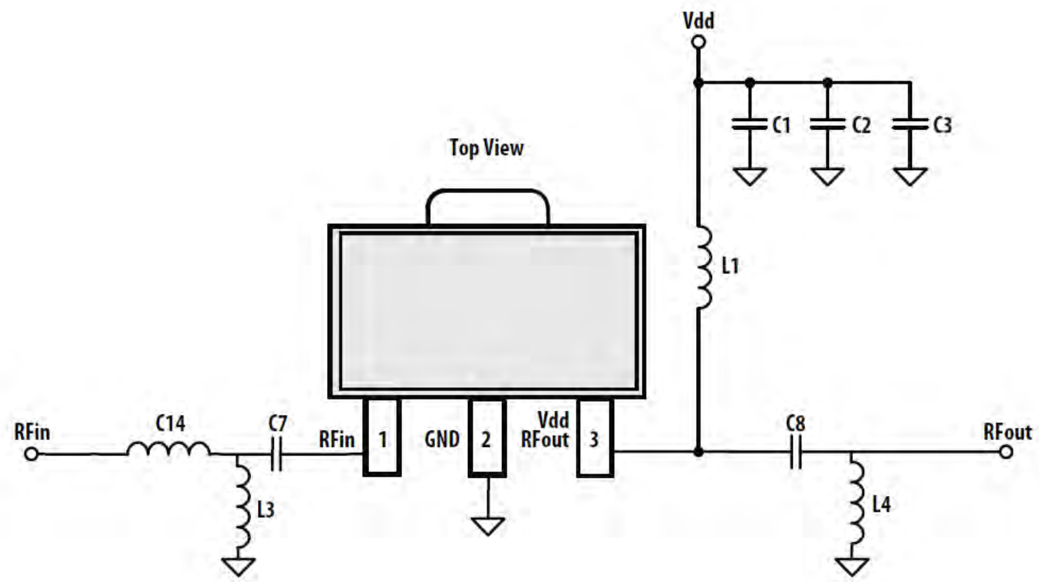


Figure 4.5: Application circuit of MGA30789 [84].

Similar to ADL5602, the +5 Volt DC biasing is supplied through the bias inductor (L_1) to the output RF port of the amplifier and the power supply is decoupled using ($C_1, C_2,$ and C_3) to reject the power supply noise. A typical DC current consumption of 100 mA is reported for this amplifier. The recommended components and application circuits of MGA30789 vary depending on the frequency range of the intended application. Table 4.2 and Table 4.3 represent the utilized surface mount lumped components for MGA30789 to be used in the TX and LO channels, respectively.

4.1.2.1 MGA30789 Impedance Matching and Co-Simulation (TX Channel)

The ADS co-simulation of MGA30789 for the TX channel is depicted in Figure 4.6. As it is shown, the amplifier's S-parameters along with the passive components' models were added to the created EM model of the layout. It is noted that the stepped-impedance was just applied at the output RF port of the amplifier to achieve the required matched responses. This was achieved by having a change in the width of the microstrip transmission line (from 2 mm to 1.156 mm) at the output RF port of the amplifier.

The operation frequency range of this amplifier is 3.04-3.64 GHz. The results of the above co-simulation along with the datasheet S-parameters of the MGA30789 amplifier are plotted in Figure 4.7. Although the S11 matched response is deteriorated compared to the S11 response of the datasheet, it is still below the standard -10 dB. Further optimization is necessary in order to shift the deep notch of the S11 at 2.75 GHz towards the operation frequency of this amplifier. However, the gain (S21), the reverse isolation (S12), and the output return loss (S22) are approximately similar to the datasheet response of the amplifier at the frequencies of interest.

Table 4.2: Utilized lumped components for MGA30789 amplifier for TX channel.

Component Ref	Datasheet Requirement	Utilized off-the-shelf Value	Unit	Size
C_1	100	100	pF	1005 (0402)
C_2	0.1	0.1	µF	2012 (0805)
C_3	2.2	2.2	µF	2012 (0805)
C_{14}	NA	NA	NA	NA
L_3	NA	NA	NA	NA
C_7	10	10	pF	1005 (0402)
C_8	5.6	5	pF	1608 (0603)
L_4	100	100	nH	1005 (0402)
L_1	4.7	4.7	nH	1608 (0603)

Table 4.3: Utilized lumped components for MGA30789 amplifier for LO channel.

Component Ref	Datasheet Requirement	Utilized off-the-shelf Value	Unit	Size
C_1	100	100	pF	1005 (0402)
C_2	0.1	0.1	µF	2012 (0805)
C_3	2.2	2.2	µF	2012 (0805)
C_{14}	NA	NA	NA	NA
L_3	4.7	330* 100**	nH	1005 (0402)
C_7	2.2	2.2	pF	2012 (0805)
C_8	2.2	2.2	pF	2012 (0805)
L_4	NA	NA	NA	NA
L_1	5.1	5.1	nH	1608 (0603)

* For Q_4, ** For Q_5

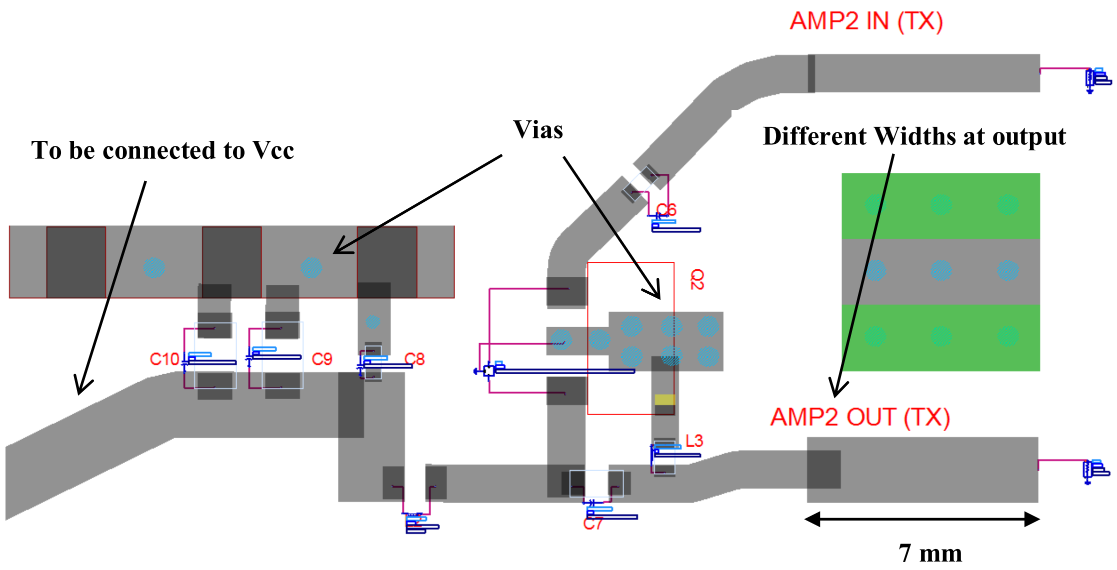
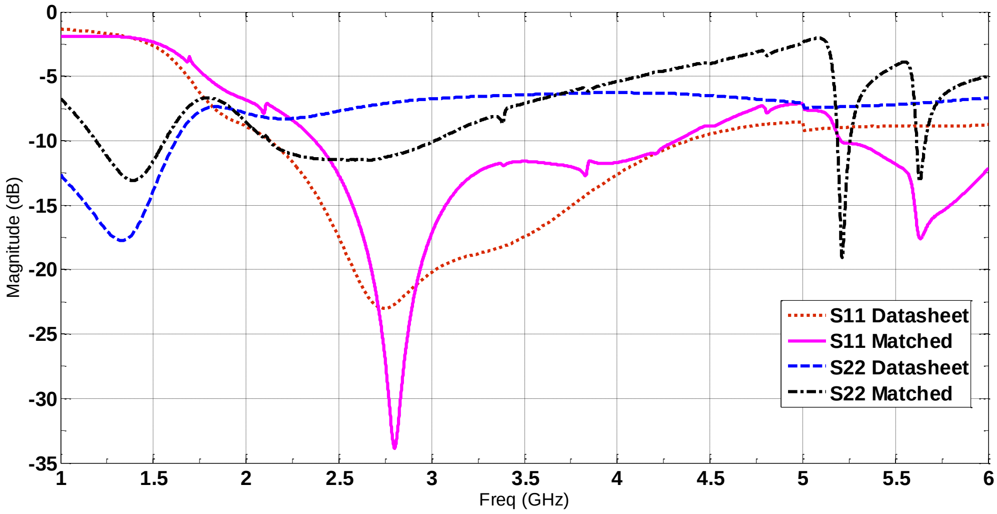


Figure 4.6: ADS co-simulation of MGA30789 for TX channel, Q2.

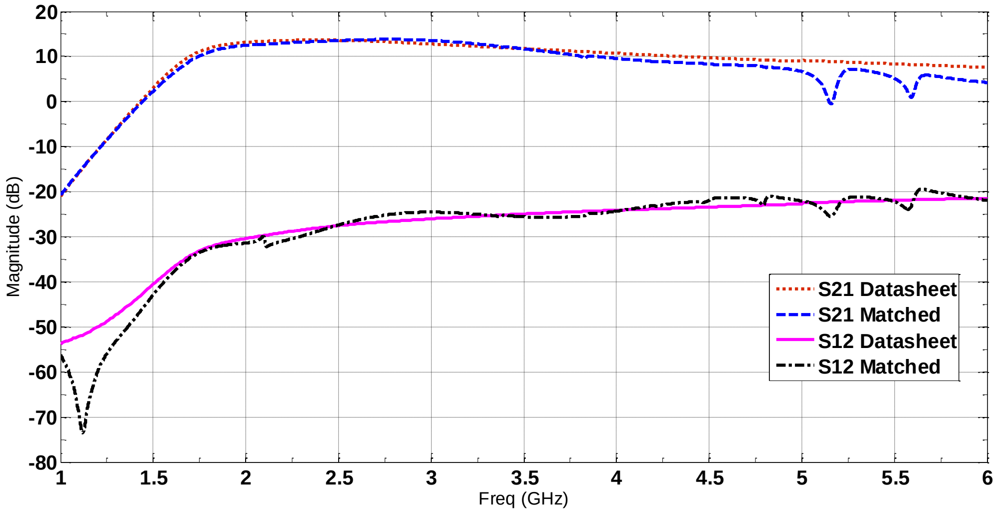
4.1.2.2 MGA30789 Impedance Matching and Co-Simulation (LO Channel)

Figure 4.8 presents the co-simulation of the two MGA30789 amplifiers (Q4 and Q5) for the LO channel of the radar's PCB. While a single width microstrip line was used for the input and output RF ports of Q4, the stepped-impedance architecture was found to be useful in enhancing the matched response of Q5 in this configuration. For this purpose, microstrip transmission lines with different widths of 1.5 mm and 1.164 mm for the input RF port and 2 mm and 1.164 mm for the output RF port were utilized.

The comparison responses of the Q4 and Q5 co-simulation along with the provided datasheet responses of the MGA30789 are presented in Figure 4.9 and Figure 4.10, respectively. These amplifiers are intended to operate in the frequency band of 3.8-4.4 GHz for the radar system. The matched responses of both amplifiers are further improved in the desired frequency band compared to their datasheet responses. The matched S11 (input return loss) is enhanced to reach -20 dB and -15 dB for the Q4 and Q5 amplifiers, respectively. Hence, the impedance matching at the input of the amplifiers was done perfectly and the amount of signal reflection at these input ports was minimized. The matched S22 of both amplifiers was also improved compared to the datasheet output return loss response. Similar to the previous amplifiers, the gain (S21) and the reverse isolation (S12) of both amplifiers follow the same trend as the ones provided in the datasheet.



(a)



(b)

Figure 4.7: Datasheet vs. matched co-simulation S-parameter responses of MGA30789 for TX channel.

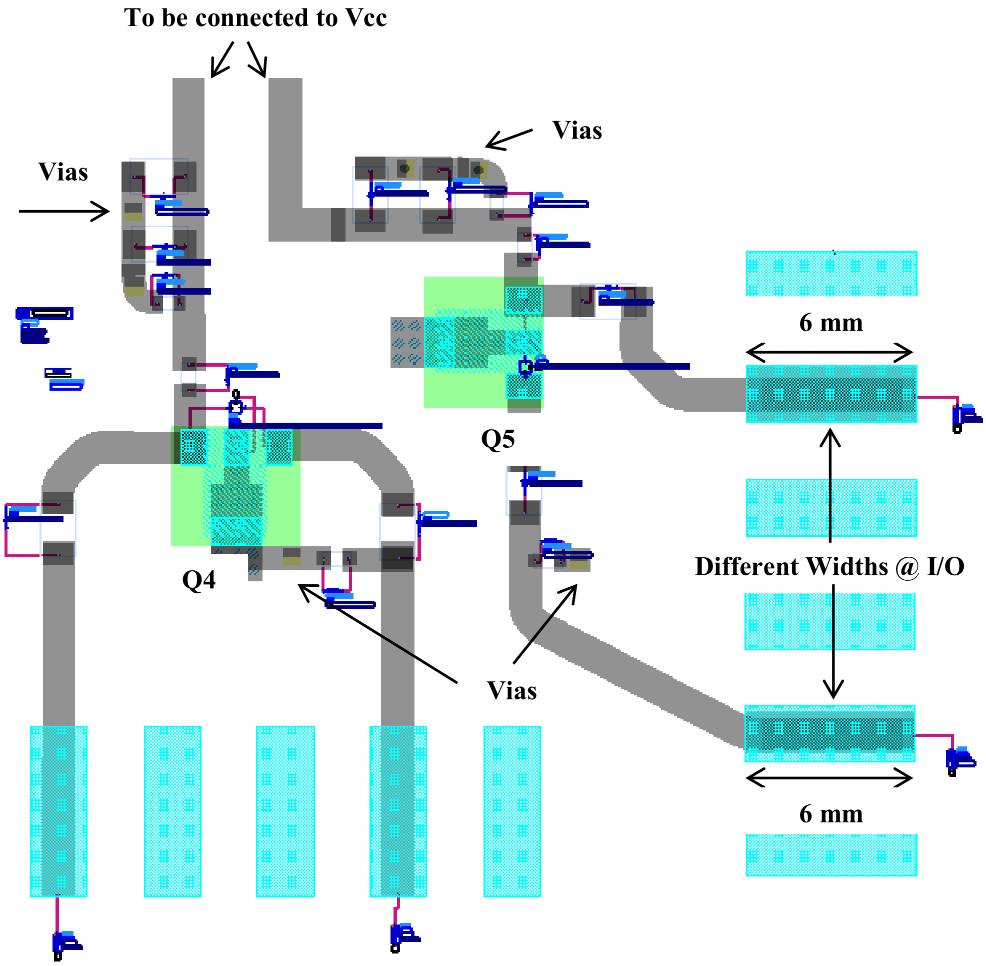
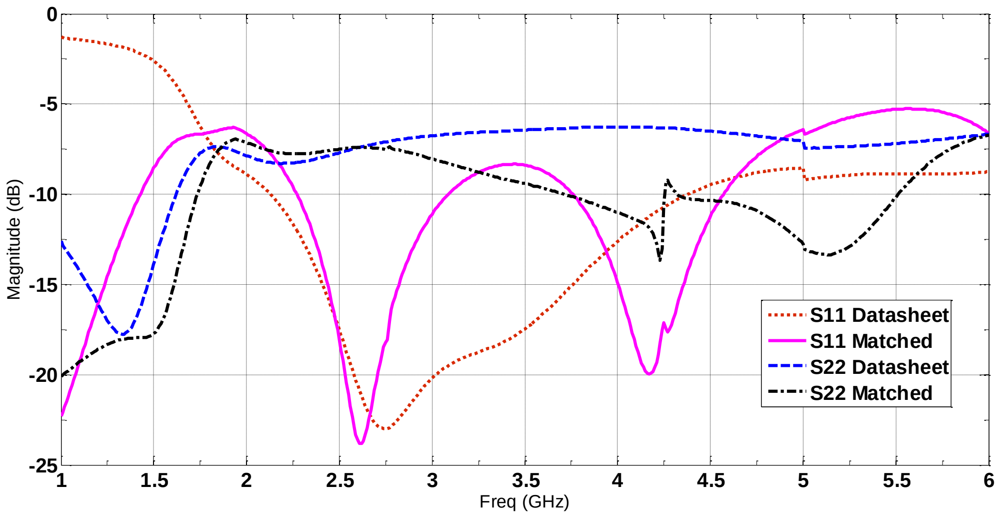
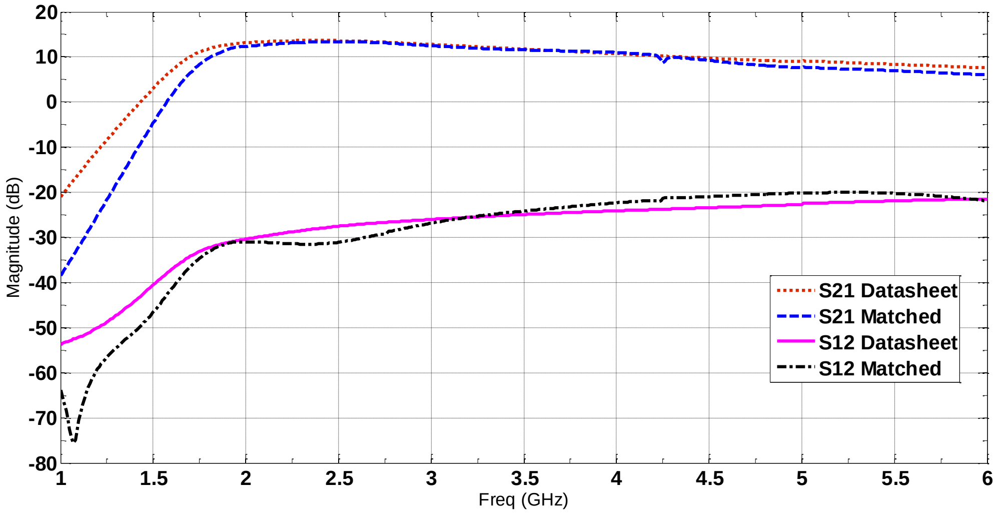


Figure 4.8: ADS co-simulation of MGA30789 for LO channel, Q4 and Q5.

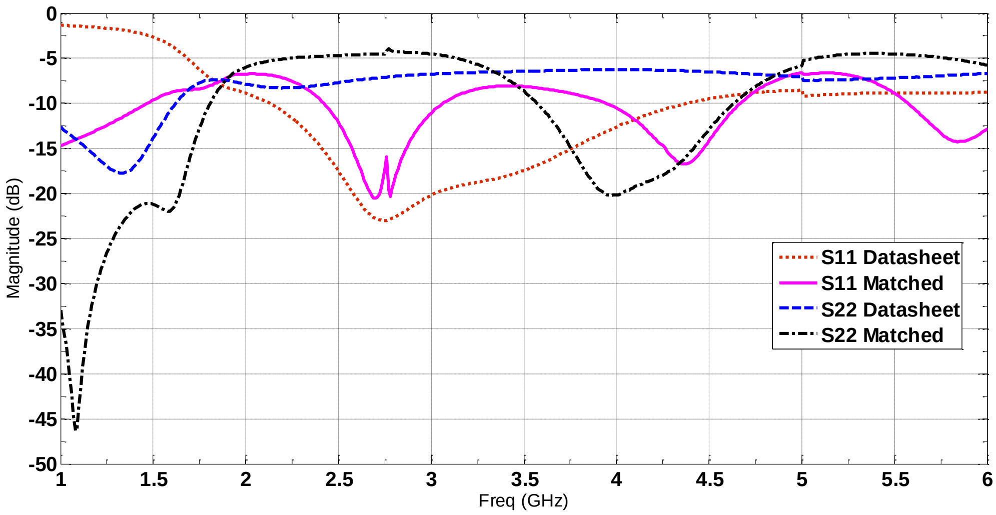


(a)

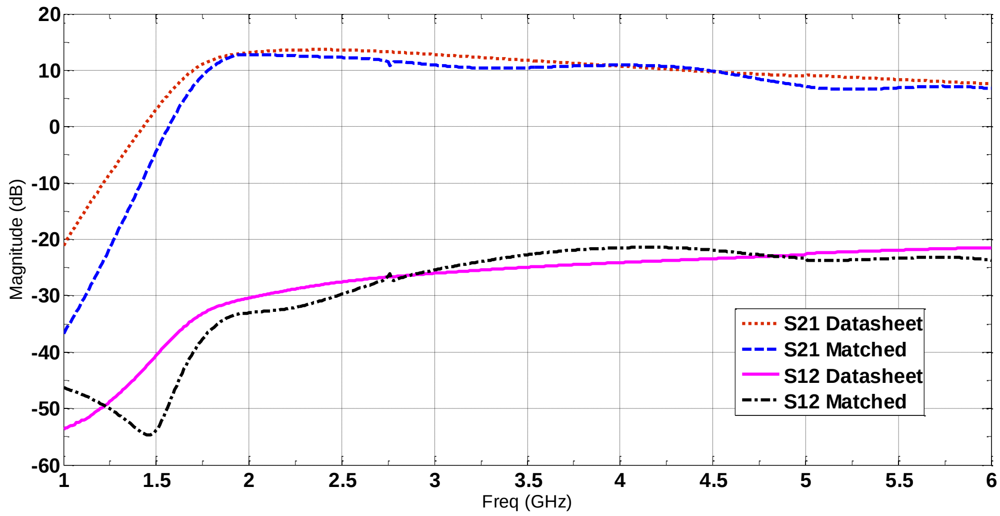


(b)

Figure 4.9: Datasheet vs. matched co-simulation S-parameter responses of MGA30789 for LO channel, Q4.



(a)



(b)

Figure 4.10: Datasheet vs. matched co-simulation S-parameter responses of MGA30789 for LO channel, Q5.

4.1.3 Amplifiers for RX Channels

The selected high linearity RFMD SBB1089Z amplifier for RX channels utilizes a Darlington configuration and provides stable current over temperature variations. The amplifier requires a +5 Volt single DC power supply and consumes 90 mA under typical conditions. The application schematic of SBB1089Z provided in its datasheet [85] is shown in Figure 4.11 below.

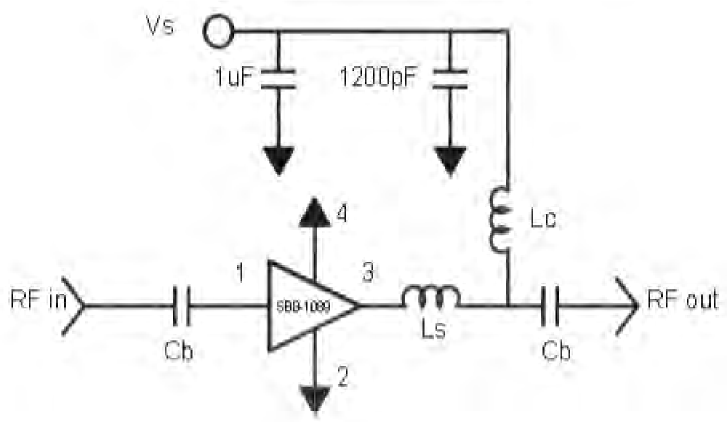


Figure 4.11: Application circuit of SBB1089Z [85].

Similar to the previous amplifiers of the TX-LO channel, the DC biasing of SBB1089Z is done through the bias inductor L_c to its output RF port. The DC supply variation (noise) is decoupled by the use of 1 μF and 1200 pF capacitors. DC blocking capacitors (C_b) are connected to the I/O RF ports of the amplifier for proper operation. Table 4.4 presents the utilized passive components for SBB1089Z along with their manufacturers and sizes. The datasheet S-parameters' response of SBB1089Z is provided in Figure 4.12. As it is seen, the SBB1089Z offers a constant gain (S21) of 15 dB and high reverse isolation (S12) over its entire frequency ranges of operation. Moreover, the input and output return losses of the amplifier are well below the standard -10 dB. This means that the input and output impedances of this amplifier are perfectly matched to 50 Ω and the amplifier functions perfectly without the need for any external matching circuitry.

Table 4.4: Utilized lumped components for SBB1089Z amplifier.

Component Ref	Datasheet Requirement	Utilized off-the-shelf Value	Unit	Size
C_b	8200	8200	pF	2012 (0805)
L_c	1.5	1.5	μH	2012 (0805)
L_s	2.7	2.7	nH	1005 (0402)
C_1	1	1	μF	2012 (0805)
C_2	1200	1200	pF	2012 (0805)

As discussed in Chapter 2, the operation frequency of the receiver channels is below 1 GHz and the down-conversion is done by means of two-stage down-conversion mixing to avoid strong in-band IMDs. The operation frequency of each down-conversion stage is 750-770 MHz and 62-78 MHz, respectively. Hence, SBB1089Z was a proper selection for both down-conversion stages of the receivers.

4.2 Frequency Doublers and Co-Simulation

The CSFD25 surface mount frequency doubler of MA-COM Technology Solutions was selected for the second up-converter stages of the TX and LO channels. The input range of this passive bridge diode frequency doubler is from 10-2400 MHz, making it suitable for both TX and LO channels of the radar system. CSFD25 utilizes four Schottcky diodes along with baluns in order to transform the internal differential design into a single-ended one at the I/O ports of the IC. The input and output impedances of CSFD25 are internally matched to 50 Ω over the entire range of operation. However, co-simulations were performed to ensure proper operation of the microstrip transmission lines, used to connect the IC to the SMA connectors at the PCB edge, at the desired frequencies. In Figure 4.13 (a), the created layout PAD for the frequency doubler of the TX channel is shown. In Figure 4.13 (b), the co-simulation of the circuit in which the frequency doubler is going to be soldered for the LO channel is presented.

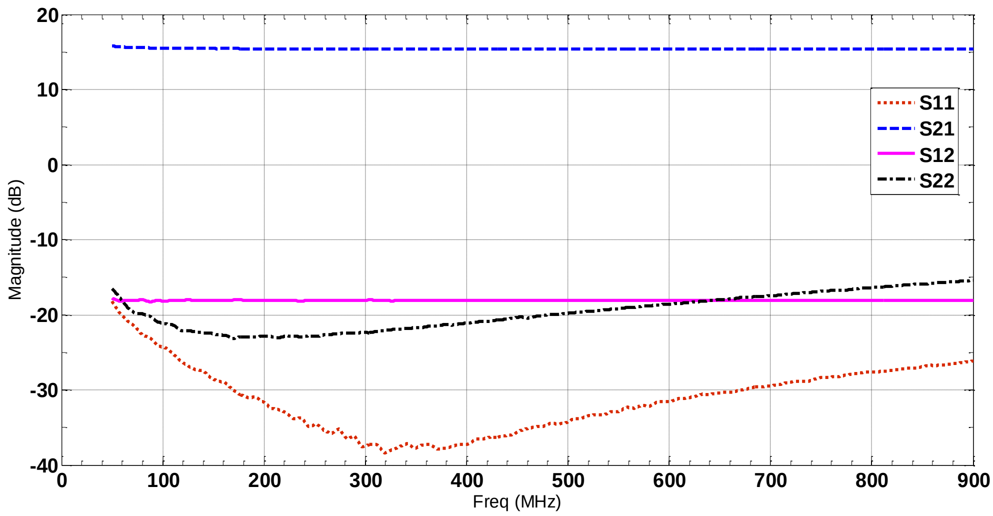
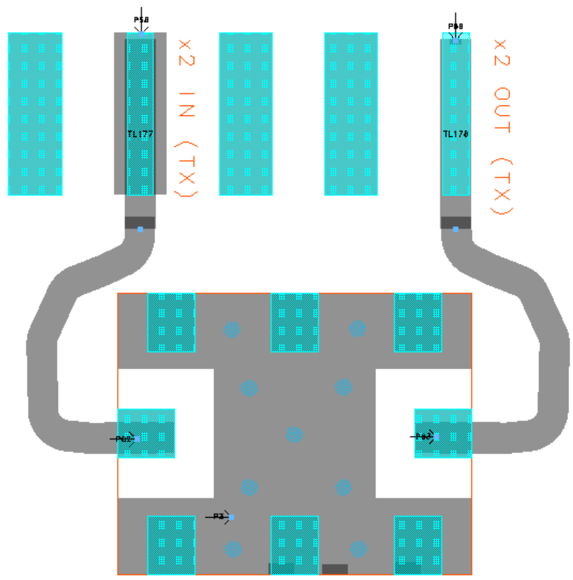
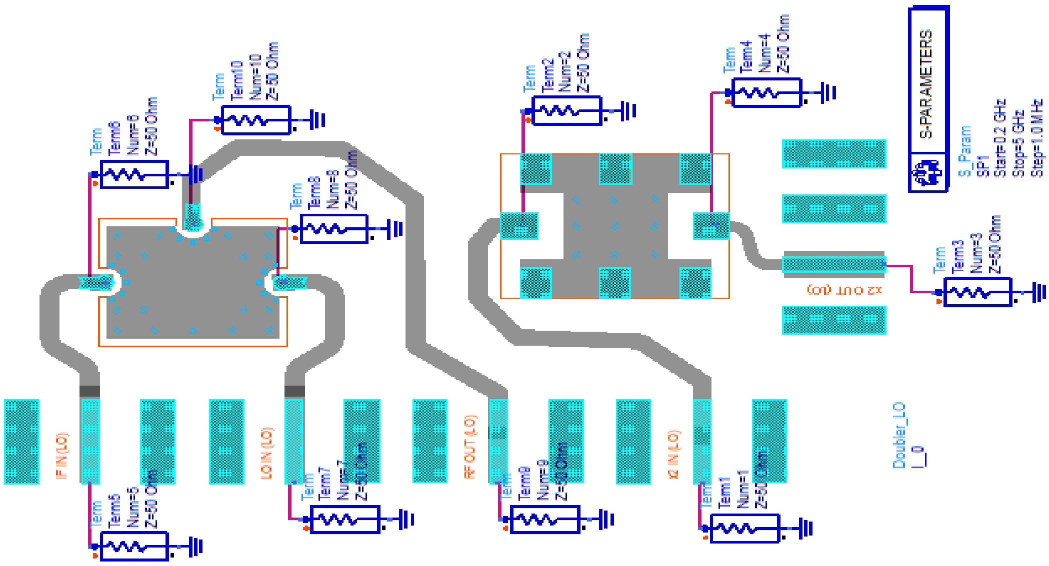


Figure 4.12: Datasheet S-parameter responses of SBB1089Z.



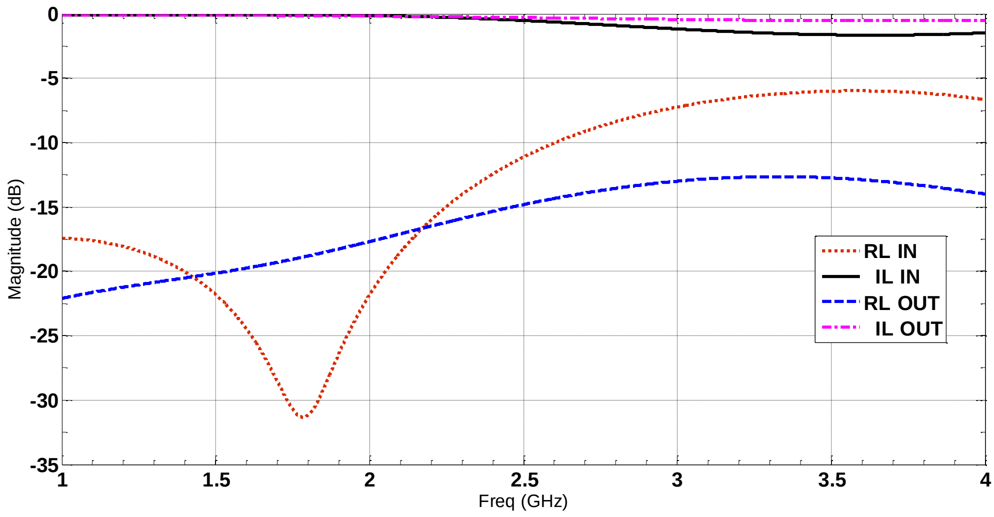
(a)



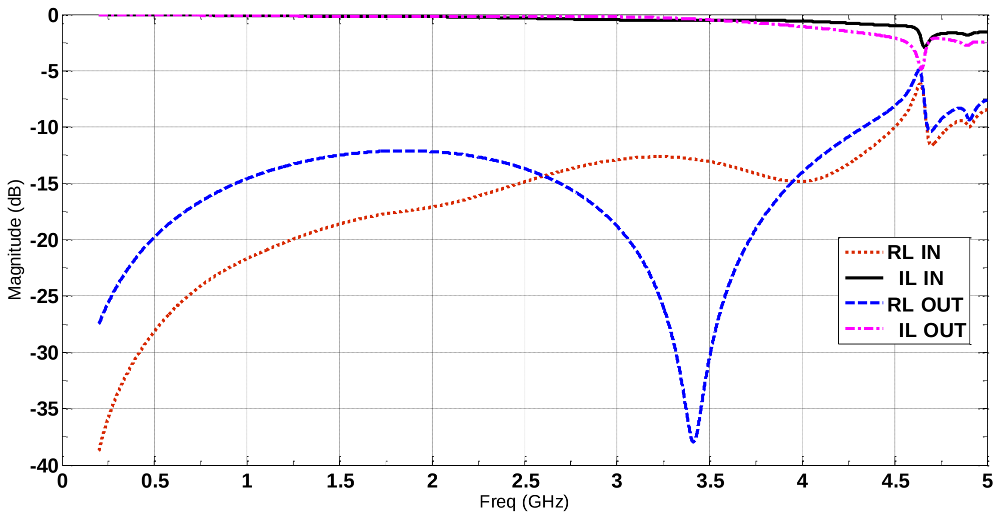
(b)

Figure 4.13: Frequency doubler PADs (a) TX channel “layout” (b) LO channel “co-simulation” with mixer’s PAD.

From Figure 4.13 (b), it is noted that 50 Ω terminations were used instead of the frequency doubler model in co-simulation. The optimal widths of the input microstrip line of the frequency doubler in the TX channel were found to be 2 mm and 1.156 mm. The widths of the input microstrip line of the frequency doubler in the LO channel was found to be 2 mm and 0.8 mm. However, the widths of the output microstrip lines were found to be 1.156 mm and 1.149 mm for the frequency doublers of both channels. The co-simulation results of the frequency doublers of the TX and LO channels are shown in Figure 4.14 (a) and (b), respectively. According to these plots, the input and output return losses of the transmission lines are below -10 dB at the desired input and output frequency ranges of both channels. The insertion losses of all utilized microstrip lines are very low indicating low loss in the transmission lines.



(a)



(b)

Figure 4.14: Co-simulation results of frequency doublers (a) TX channel (b) LO channel.

4.3 Typical Mixer and Co-Simulation

Passive surface mount T3-05 Marki Microwave mixers were used as the required mixers of the radar's PCB testbed. These mixers are high-performance nonlinear mixers with good spurious performance operating in a wide range of frequencies from 1 MHz up to 5 GHz for RF/LO and 1 MHz to 4 GHz for the IF port. The impedance of the mixer ports are AC matched to 50 Ω eliminating the need for any external circuitry for impedance matching purposes. Similar to the frequency doublers, co-simulations were performed for all the utilized transmission lines for the mixers (with PAD) of the radar's PCB testbed. As a typical example, Figure 4.13 (b) shows the co-simulation of the mixer to be soldered on the PCB for the LO channel. This typical example is shown due to the close spacing of the mixer's IF track with the input track of the frequency doubler. The PAD's dimension of the mixer was provided by the manufacturer and was inserted into the layout. The widths of the microstrip lines at the center frequency of operation were calculated using LineCalc. Figure 4.15 shows the typical co-simulation results of three microstrip lines to be connected to the mixer when loaded with 50 Ω terminations. As it is shown, the return losses of all three microstrip transmission lines are below the standard -10 dB at the desired frequencies. The insertion losses are very low such that they are not obvious in the graph.

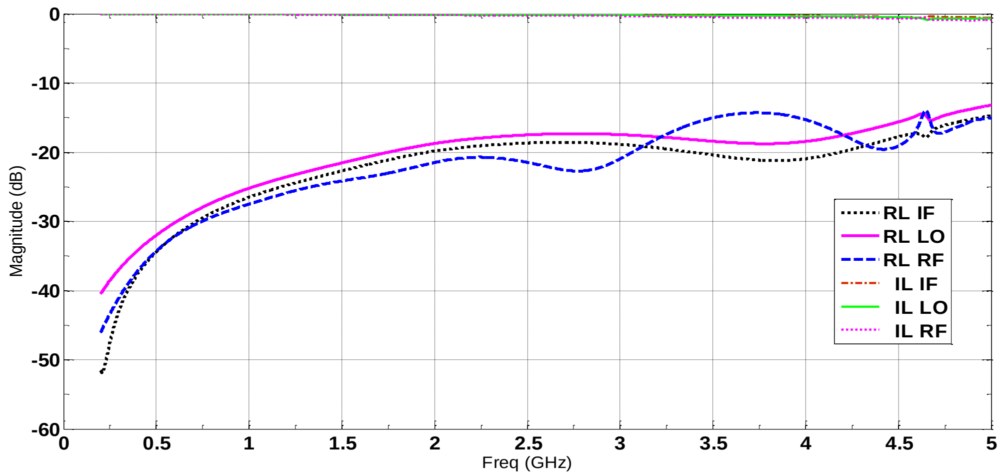


Figure 4.15: Typical co-simulation responses of the microstrip transmission lines for the mixers.

4.4 Radar's PCB Integration

After optimization and simulation of each individual block, the integration of individual radars' stages on a single PCB was the next task. The PCB integration was to be carried out in a way which maximized accessibility and eased the testing procedures of the individual stages. In order to ensure the ease of individual testing, the radar system's components were not cascaded on the PCB prototype. This would allow for easier component replacement should any design malfunctions be discovered. This method then required each stage to have its individual I/O RF SMA connector. In addition, two separate PCBs were required to be fabricated for the TX-LO channel and array of RX channels. The design and development of each PCB for the radar testbed is discussed in the following section.

4.4.1 TX-LO Channel PCB

A single PCB was intended to be fabricated for the TX and LO channels. The TX channel consists of six cascaded blocks which are a mixer and a frequency doubler to up-convert the input chirp, two filters to reject the undesired spurious products, and two amplifiers in order to increase the power level of the up-converted signals. The LO channel consists of the same components as the TX channel with an additional amplifier at the output stage to increase the power level of the up-converted signal to a level suitable for the drive requirements of the receiver's mixer. The difference between the two channels is in their operating frequencies as discussed in Chapter 2. Hence, the TX-LO PCB consists of 13 different stages in which 11 stages have two I/O ports and the other two (mixers) require three ports (RF, LO, and IF). Hence, a total of 28 RF SMA connectors are required in order to place each stage independently without cascading them.

Each SMA connector occupied 1 cm with 2 mm spacing between itself and the next. Therefore, for a four-sided PCB with a total of 28 SMA connectors, seven connectors were placed on each side. Hence, the minimum required length of each side of the PCB was determined to be 8.2 cm. Another important factor was to place all the stages of the TX-LO channels next to each other without the overlap of the required I/O tracks for external connections. Figure 4.16 shows the developed layout for the TX-LO channels' PCB. The black areas represent the top conductor layer of the PCB and the white areas represent the locations of bare conductors (where it is not desired to place a solder mask). All the ground planes on the top layer of the PCB were connected to its bottom conductor layer (which is not shown in the figure) through via holes. The entire bottom conductor layer's purpose is to serve as a large ground plane in order to minimize the thermal impedance and provide a ground path for the RF waves as well as the DC currents of the amplifiers. The green areas represent the bare conductor locations of the bottom conductor layer where the SMA connectors are to be soldered. In Figure 4.16, red is used for text annotations and to outline the positions of ICs to be soldered on the board. The overall size of the TX-LO PCB is $10.6 \times 9.6\ cm^2$.

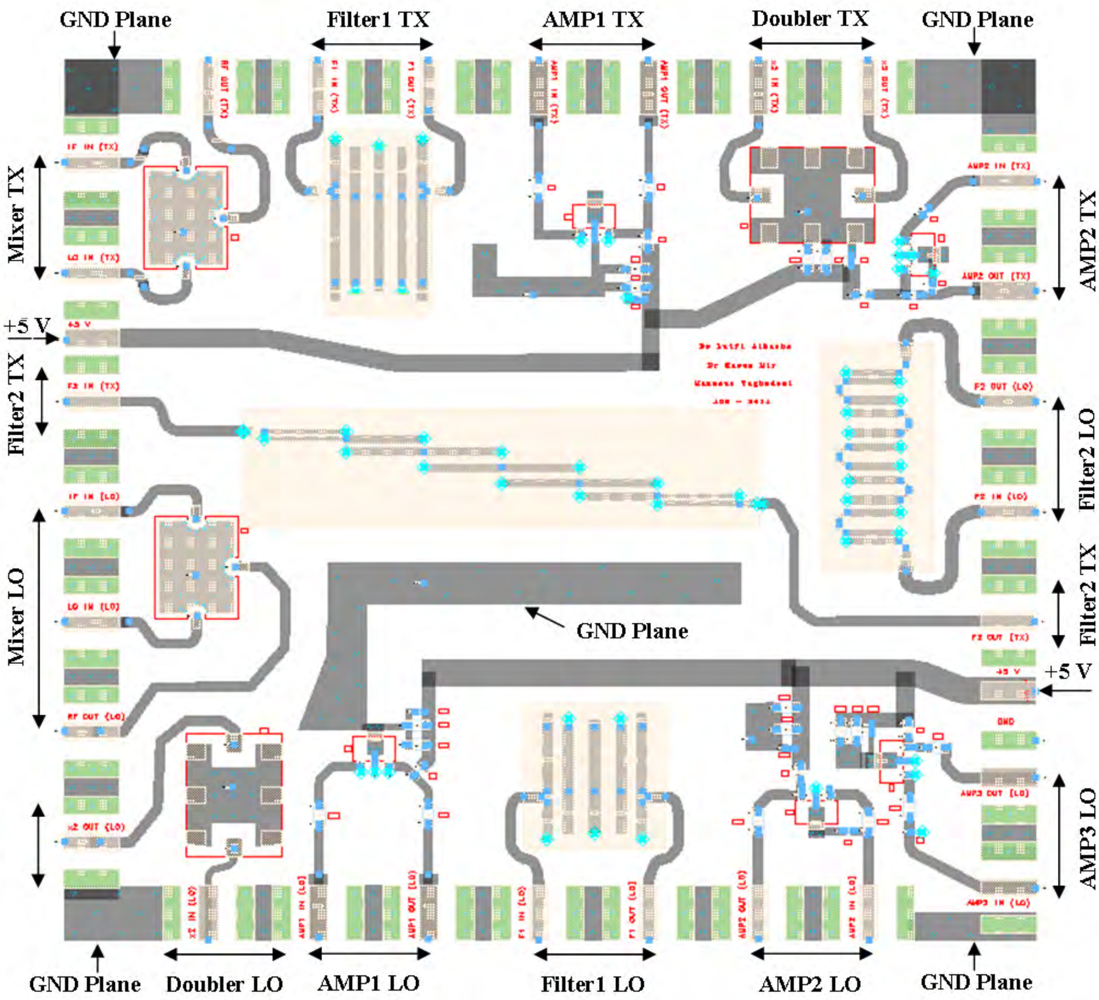


Figure 4.16: Layout of TX-LO PCB.

Different stages of TX and LO channels are labeled on Figure 4.16. Evidently, the TX channel's stages were placed at the top half of the board and the LO channel's stages were positioned at the bottom half to isolate the two channels. The major obstacle in the design of the TX-LO PCB was the large coupled line filter intended for the second filtering stage of the TX channel. Two distinct +5 Volt tracks were specified to separate the DC biasing of the amplifiers for the two channels. The widths of the tracks were specified based on the overall DC current requirements of the amplifiers to reduce the I-R voltage drop as much as possible.

As mentioned in the impedance matching section, the widths of the I/O tracks for the mixers and doublers were calculated at the desired center frequency of operation. The symmetry in the critical tracks such as the RF and LO paths of the mixers were maintained to avoid phase mismatches. The widths of the amplifiers' I/O tracks were discussed in the impedance matching section. The empty spaces on the top layer of the board were filled with a ground plane which was connected to the bottom ground layer through grounding via holes. The large ground plane on the top layer of the board provided isolation between the circuits at the top and bottom sections of the PCB.

Solder masks were added to the boards in order to protect the fabricated copper patches and tracks. As it is shown in Figure 4.16, the coupled microstrip lines of the filters were covered with white rectangular patches to have bare microstrip lines without any solder masks on top of them. By placing solder masks on the top of these coupled microstrip lines, the amount of coupling between the microstrip lines is affected. Hence, this results in low performance and degradation in terms of filters' responses. In addition, the required via holes for the interdigital filters were changed to two 6.5 mils vias instead of a single 13 mils via after consulting with the fabrication company. After finalizing the layout design, the overall TX-LO PCB was simulated using co-simulation in ADS. The comparison of the simulation results versus measurements of different stages are provided in the next chapter.

4.4.2 RX Channels PCB

The radar system was aimed to have an array of receiver channels in order to perform several tasks such as adaptive beamforming, spatial filtering, and tracking specific targets in a certain direction of interest. To do so, the same receiver channel is to be replicated in order to be positioned in different angles to change the arrival angles of the transmitted signals. Hence, it was decided to integrate two receiver channels on the same RX PCB for the PCB prototype of the radar system.

Each receiver channel consists of two down-conversion stages. Each stage consists of a surface mount T3-05 mixer, a BPF, and an amplifier. Figure 4.17 depicts the developed layout for the RX PCB with the two RX channels. The dashed line in the center of the layout determines the border of the two RX channels. These two RX channels are the replica of each other and were placed with 180° rotation in order to reduce the overall size of the board as much as possible. Two separate power supply tracks (+5 Volt) were positioned on the PCB in order to turn on the required RX channel whenever necessary. The required width of the supply tracks was calculated based on the maximum current consumption of the two amplifiers to avoid a voltage drop in the supply path. Similar to the layout of TX-LO PCB, the black areas represent the top conductor layer of the board while the white areas on the top of the conductors indicate the location of bare copper without the solder mask. The red annotations indicate labeling and components' outlines and the green areas represent the bare copper on the bottom conductor layer of the PCB.

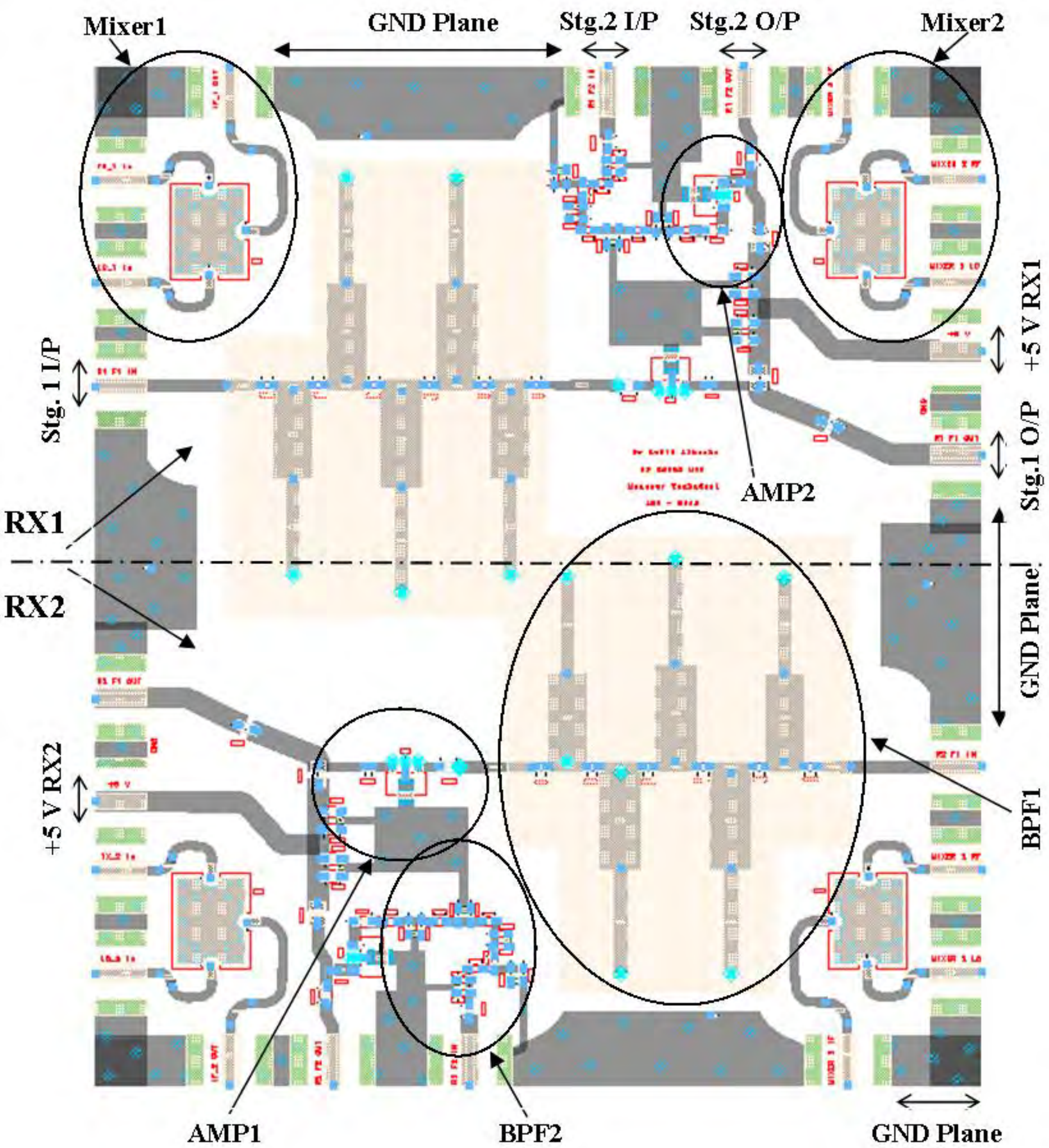


Figure 4.17: Layout of RX PCB.

As the operation frequency of the RX channels is low and a high performance amplifier was utilized, it was decided to cascade the filter and the amplifier of each down-converter stage on the board. Hence, the number of SMA connectors was reduced by 30% which reduced the overall cost, size, and complexity of the RX board as well. As labeled on Figure 4.17, each RX channel consists of two mixers in which symmetry was maintained in their RF and LO paths to avoid phase mismatches. The widths of these microstrip lines were calculated at the center frequency of the intended band of operation for each mixer. Other stages of each down-converter (BPFs and amplifiers) are also labeled on the PCB layout of the RX channels. The empty spaces on the margins of the PCB were filled with ground planes which were connected to the bottom ground layer of the board through via holes. These ground patches help in having necessary ground paths for the I/O RF signals through SMA connectors when soldered to the PCB edge. In addition, large ground planes were added close to the amplifiers in order to provide enough DC current paths to the bottom ground plane and reduce the overall thermal impedance by dissipating the heat generated by the amplifiers. The design of the RX PCB was simpler compared to the TX-LO PCB due to its lower operation frequency with lower parasitic effects.

The overall size of the RX PCB is $10.4 \times 12\ \text{cm}^2$. The major issue in the design of the receiver channels was the first BPF which increased the overall size of the RX PCB. The operation frequency of this filter is not suitable for microstrip technologies which result in bulky filters. However, the size of the filter was further reduced by utilizing a hybrid combination of distributed and lumped elements. As seen in the layout of the RX PCB, the SIRs in these filters were covered by white rectangles in order to have bare copper, not covered with solder masks. While the SIRs do not operate by coupling with other microstrip lines, placing the solder mask does not harm the filter response. However, the simulation of these filters was done using bare copper and it was more secure to avoid placing solder mask on top of these SIRs. Similar to the interdigital filters of the TX-LO channels, the required grounding via holes of these filters were changed to two 6.5 mils vias instead of a single 13 mils via after consulting with the fabrication company. After finalizing the layout design of the RX PCB, the overall design was simulated using co-simulation in ADS. The comparison of the simulation results versus measurements of the two down-converter stages of the RX channels are provided in the next chapter.

Chapter 5: Measurements versus Simulation Results

After PCB fabrication, the boards were ready to be tested and evaluated for performance validation. The testing of the PCBs was done in two different phases. Initially, the functionality of each individual block was verified by means of S-parameter measurements. The measured responses were compared with the co-simulation results of the same stage when placed on the final PCB prototype. After verifying the functionality of all individual stages, the overall PCBs were tested in the radar system configuration where a single tone and LFM chirp signals were applied to the TX and LO channels and the output of the RX was analyzed. The individual block comparisons as well as the system measurement results are provided in this chapter.

Figure 5.1 and Figure 5.2 depict the fabricated PCBs for the TX-LO and RX channels of the radar testbed. As it is shown, the boards consist of 50 Ω RF SMA connectors to test individual stages. The solder mask (green) layer was added to the boards except on the filters and via holes in order to protect the copper tracks. All the required components such as the surface mount mixers, frequency doublers, amplifiers, inductors, and capacitors were soldered to the boards as well.

5.1 Measurements vs. Simulations of Individual Stages of Radar's PCBs

The performance of mixers and frequency doublers were verified by applying different signals at the inputs and measuring the output signals using a VNA spectrum analyzer. In the following section, the measurements versus co-simulation results of individual filters and amplifiers when integrated on PCBs are presented. In Figure 5.3, a typical S-parameter measurement setup is shown. This measurement setup consists of an Agilent E5071C VNA and the filter or amplifier under test (DUT). It is noted that as active elements, amplifiers were supplied with a +5 V DC power supply and the S-parameter measurement was conducted. Before the measurements, the VNA was calibrated using the calibration kit (Agilent 85033E). Each VNA port was individually calibrated for the standard open, short, and matched loads for the measurement's frequency range. Then the transmission calibration was done by shorting the two ports of the VNA together. Hence, the VNA was ready for S-parameter measurements of the individual stages of the radar's PCBs.

The S-parameter measurement of each stage in the radar system architecture was done individually. The measurement results by VNA along with the co-simulation results of the ADS simulator were transferred into MATLAB and the comparison graphs were plotted. In the following section, the measurements versus simulation results of each stage of the TX-LO and RX PCBs are presented.

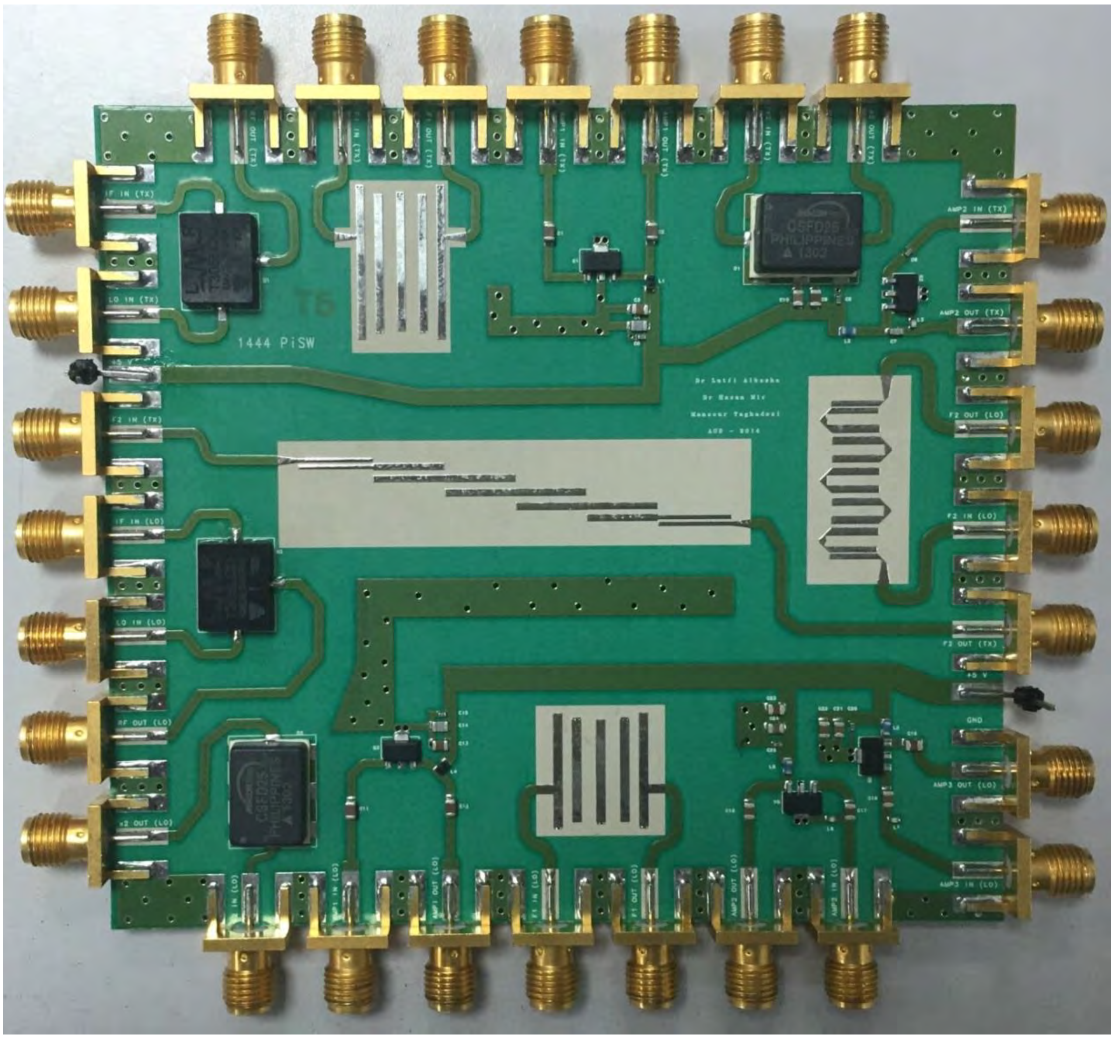


Figure 5.1: Fabricated TX-LO PCB.

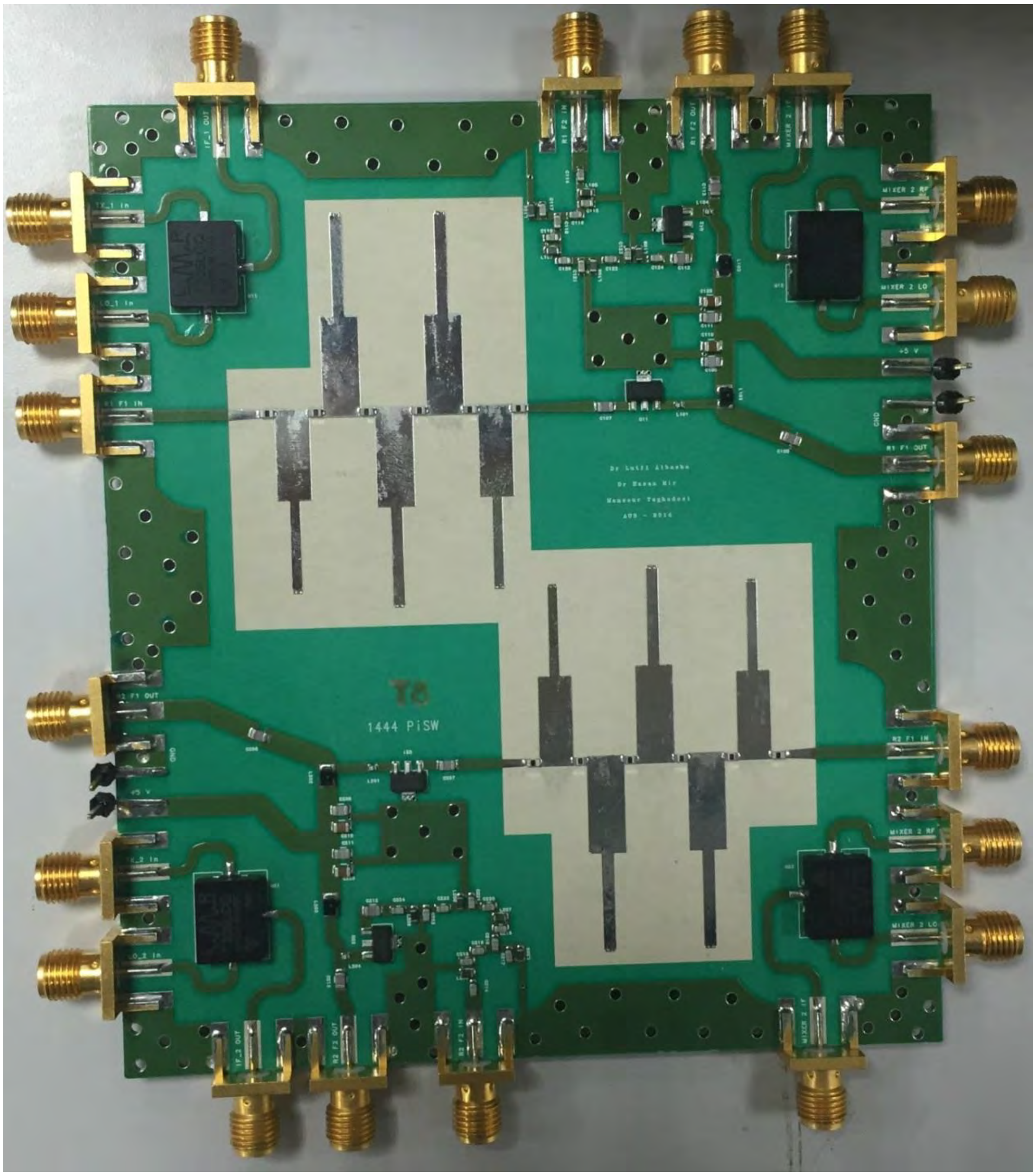


Figure 5.2: Fabricated RX PCB.

5.1.1 TX-LO PCB

The TX-LO PCB consists of four filters along with five amplifiers. The TX channel has two filters and two amplifiers whereas the LO channel has two filters and three amplifiers. First, the test and measurements of the filters and amplifiers are presented in the following sections.

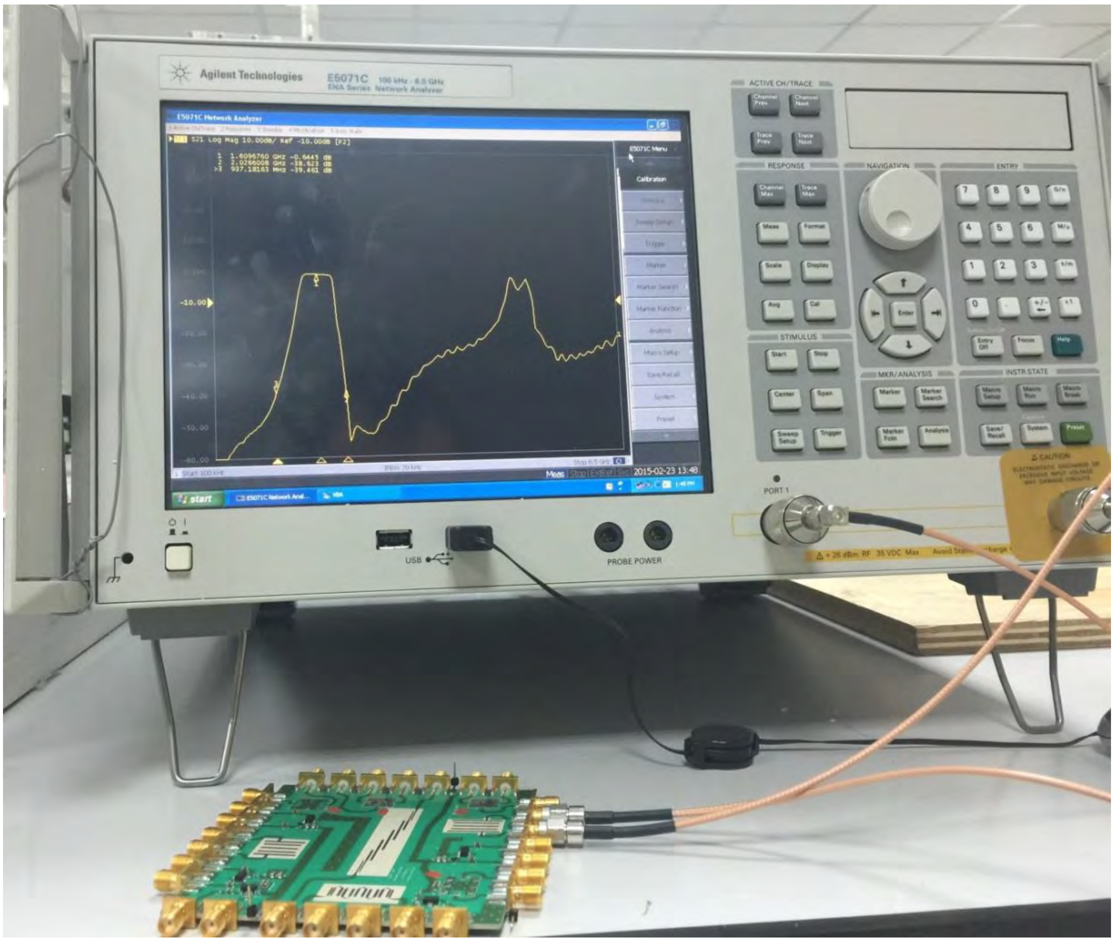


Figure 5.3: Typical S-parameter measurement setup (filter under test).

5.1.1.1 First-Stage Filters (Interdigital Filters)

The first stage filters of both the TX and LO channels are interdigital filters which were selected due to their superior spurious response compared to the other microwave filters. The measured S-parameter responses of the interdigital filters for the TX and LO channels along with their simulated responses are shown in Figure 5.4 to Figure 5.7, respectively. From these plots, the measured input and output return losses (S11 and S22) are very close to the simulated responses for both filters. The return loss of the first filters in the TX and LO channels are well below -20 dB and -15 dB, respectively. This is an indication of a perfect impedance match of both filters to the 50 Ω over their pass bands. Although the bandwidths of both fabricated filters are slightly increased from the lower side, the measured transmission responses (S12 and S21) for both filters follow the same trend of the simulated ones. As expected from the ADS simulations, the measured insertion losses of both filters are very low within the pass bands (-0.8 dB average). The rejection levels of the measured and simulated filters are very close to each other as well. The second harmonic of the fundamental pass bands are filtered effectively as was expected from the simulations. The first spurious responses of the filters occur at the third harmonic of the pass band which is not of major concern.

5.1.1.2 Second-Stage Filters (Parallel CL for TX Channel and Hairpin for LO Channel)

While a parallel coupled line filter was used for the second stage filtering of the TX channel, a hairpin filter was used for the LO channel due to its compact size. The measured S-parameter response of the second stage filters of the TX and LO channels along with their simulated responses are compared in Figure 5.8 to Figure 5.11, respectively. From the comparison plots, the return loss responses (S11 and S22) of both filters follow the same pattern and are nearly below -10 dB in the pass bands of both filters, indicating an acceptable impedance match to the 50 Ω. However, the return loss of the fabricated hairpin filter is a bit worse compared to its simulated response. While the insertion loss of the fabricated hairpin is constant (-1.7 dB average) compared to the introduced ripple in the simulation, the fabricated CL filter exhibits a worse performance in terms of pass band ripples compared to the simulation one. In both filters, the measured bandwidths are increased from the lower sides indicating a slight shift in the center frequencies of the filters towards lower frequencies. In addition, the upper sides of the pass bands are slightly shifted to lower frequencies. While the rejection level of the fabricated CL filter is similar to the simulated one, the hairpin filter reveals a better rejection at the lower side of the pass band compared to its simulated response.

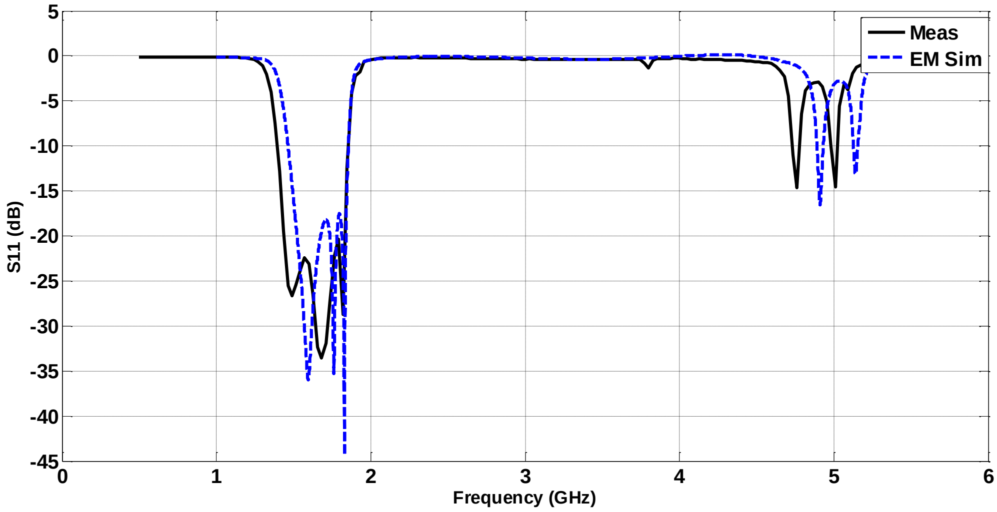
5.1.1.3 First-Stage Amplifiers (ADL5602)

ADL5602 is a high-gain block which was tripping the VNA when connected directly as a result of high power signal. Hence, a 6 dB attenuator (PAD) was used at the output of the amplifier to maintain the VNA's safety. The 6 dB attenuator at the output ports of the amplifier causes 6 dB attenuation in the output return loss (S22), the reverse isolation (S12), and the gain (S21) of the amplifier and does not affect the input return loss (S11). The comparison between the measurement's S-parameter responses of ADL5602 versus the ADS co-simulation results for the TX and LO channels' PCB are shown in Figure 5.12 to Figure 5.15, respectively. From the comparison plots, the measured return losses of both amplifiers for the two channels are below -10 dB for the intended frequency ranges and follow the same trend of the simulation responses. Hence, the signal reflections at the input ports of the amplifiers at the desired frequencies are minimized by proper impedance matching to 50 Ω. The amplifiers offer an approximate constant gain of 19 dB over the entire designated frequencies of the two channels. The measured reverse isolations of both amplifiers are high enough, as expected from the simulations. Moreover, both amplifiers exhibit better measured output return losses compared to those of simulations at desired frequency bands.

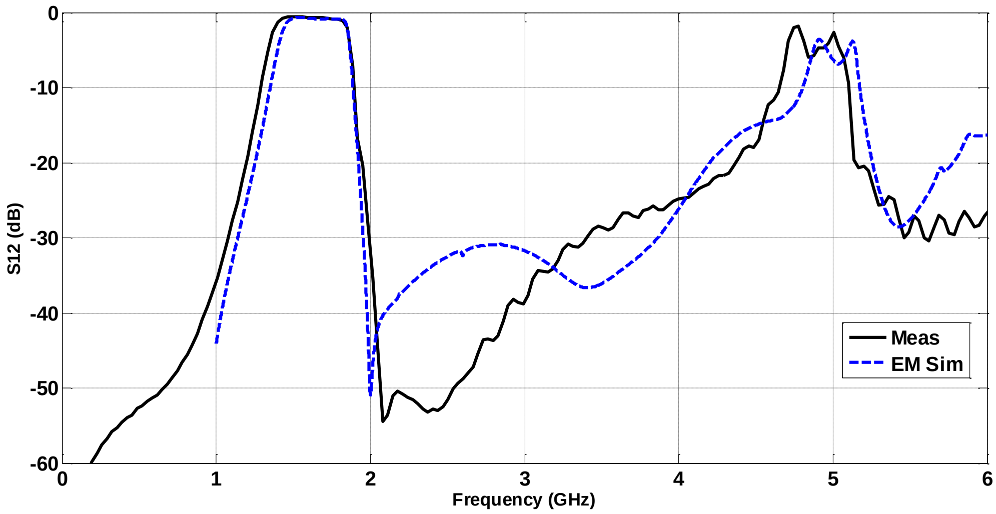
5.1.1.4 Second-Stage Amplifiers (MGA30789)

The comparison between the measurement's S-parameter responses of the MGA30789 versus the ADS co-simulation results for the TX and LO channels' PCB is shown in Figure 5.16 – Figure 5.21, respectively. From the comparison plots, it is observed that the return loss responses of all three amplifiers approximately follow the same trend as those of the simulation responses. Although the measured return loss response of the TX amplifier is well below -15 dB in the designated frequency range, the measured return loss of both LO amplifiers is degraded in the 3.8-3.9 GHz range. However, the measured return losses of both amplifiers are well below -10 dB as was expected from the simulation results. All three amplifiers offer high measured reverse isolation responses similar to the simulated ones. With the exception of a few ripples in the measured gains, the measured and simulated gains exhibit the same characteristics. The measured output return losses of all amplifiers are acceptable as they are below the standard -10 dB in the intended frequency ranges of each amplifier and follow the same trend of the simulated responses.

Filter 1 in TX channel: 1.52-1.82 GHz

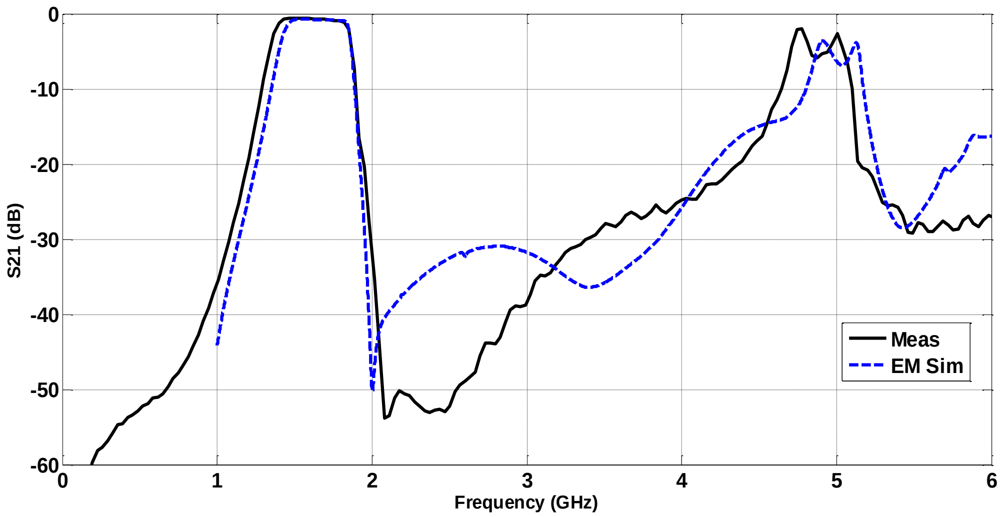


(a)

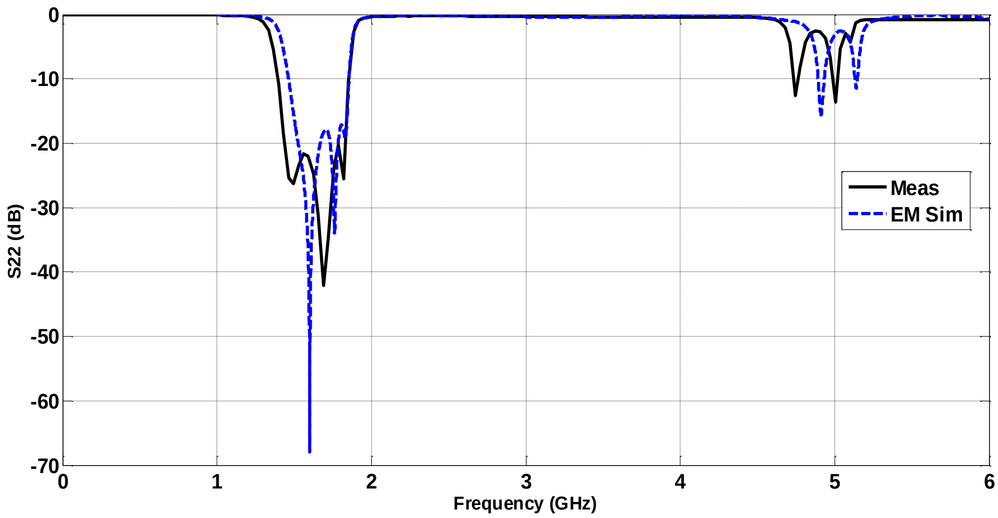


(b)

Figure 5.4: Measurements vs. EM simulation results of filter 1 in TX channel (a) S11 (b) S12.



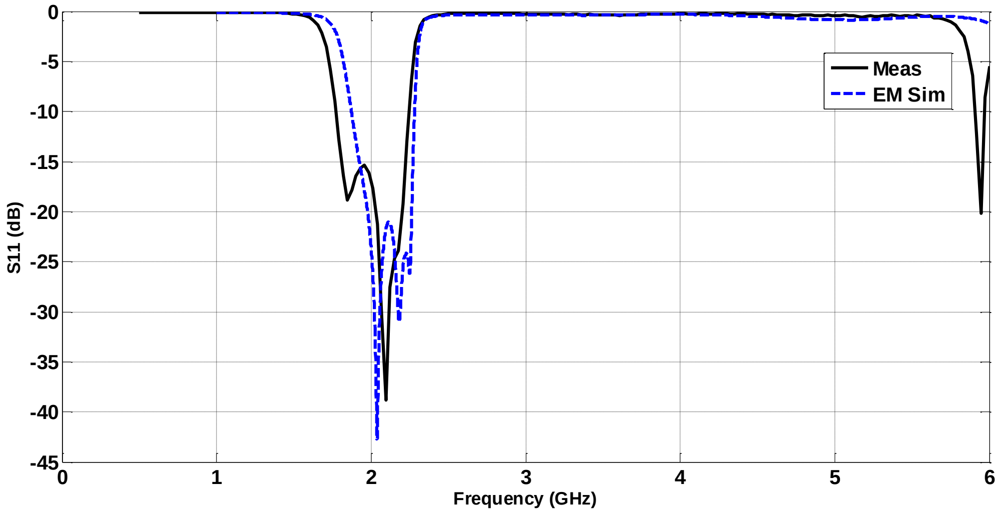
(a)



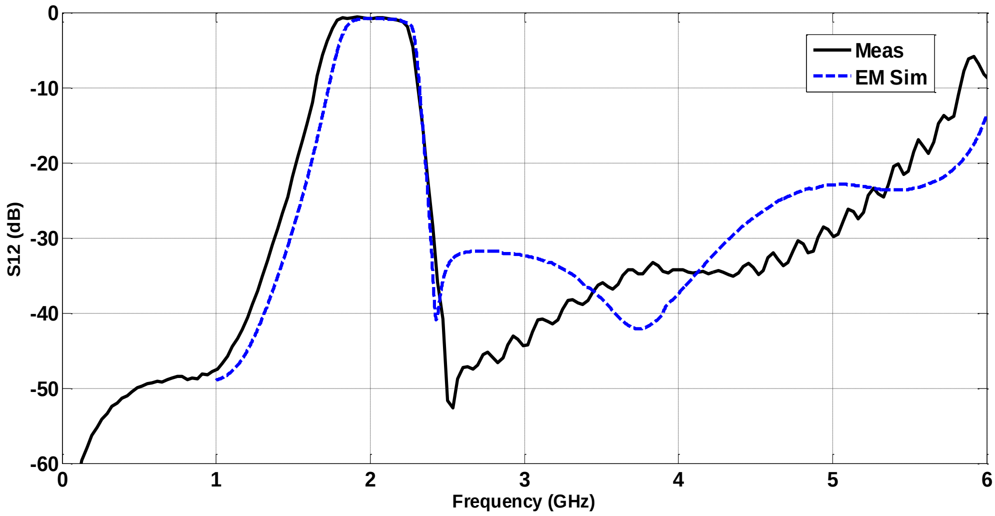
(b)

Figure 5.5: Measurements vs. EM simulation results of filter 1 in TX channel (a) S21 (b) S22.

Filter 1 in LO channel: 1.90-2.20 GHz

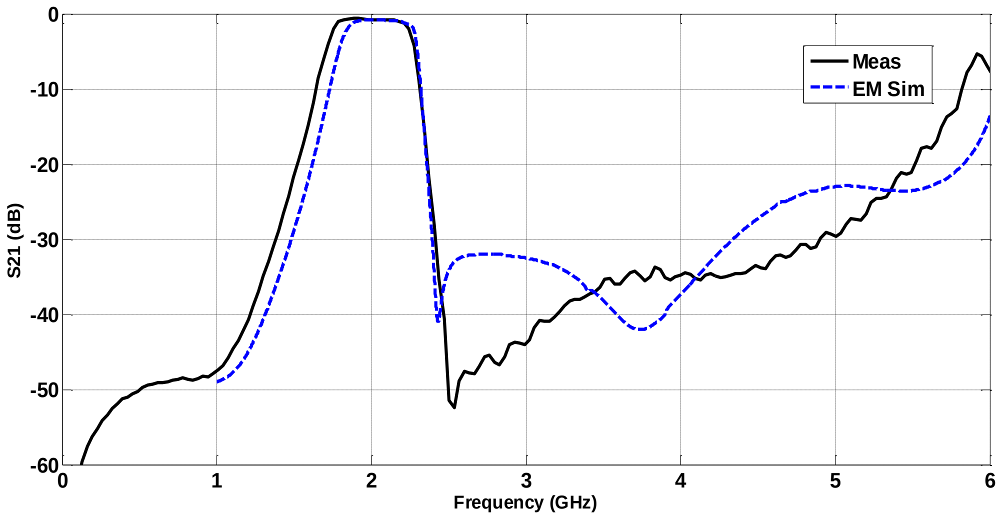


(a)

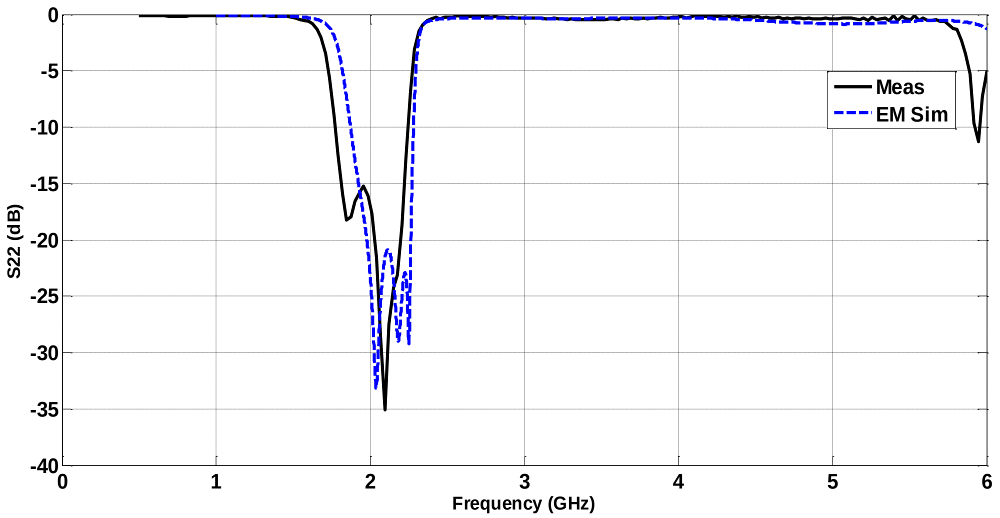


(b)

Figure 5.6: Measurements vs. EM simulation results of filter 1 in LO channel (a) S11 (b) S12.



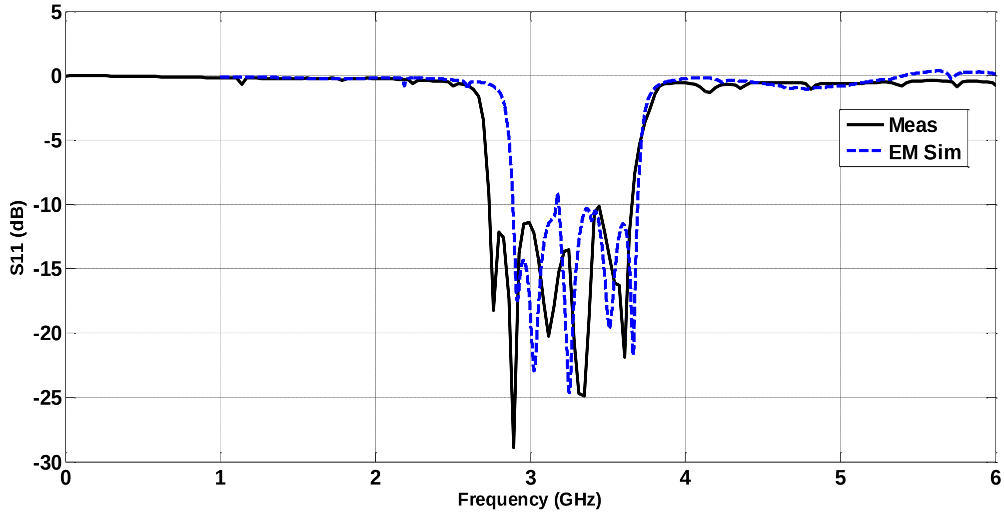
(a)



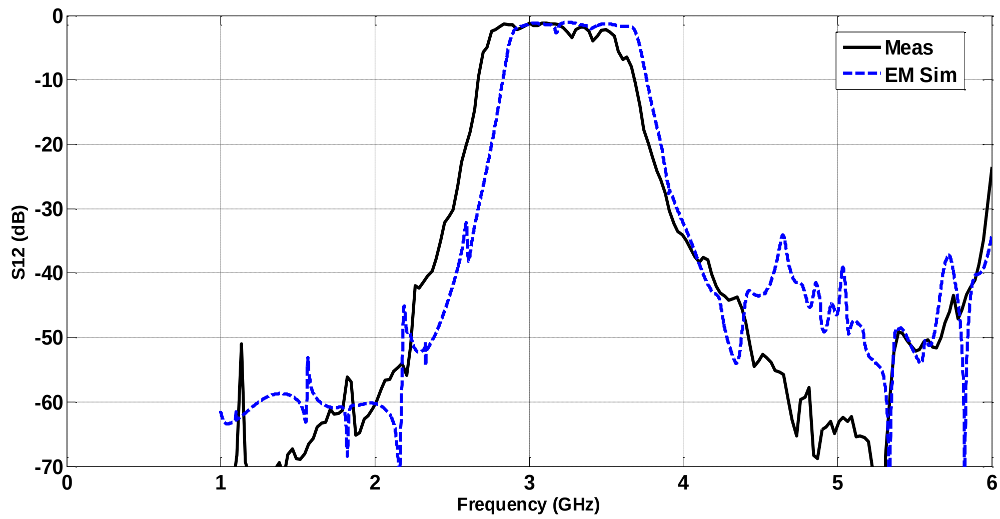
(b)

Figure 5.7: Measurements vs. EM simulation results of filter 1 in LO channel (a) S21 (b) S22.

<u>*TX Channel Filter 2: 3.04-3.64 GHz*</u>

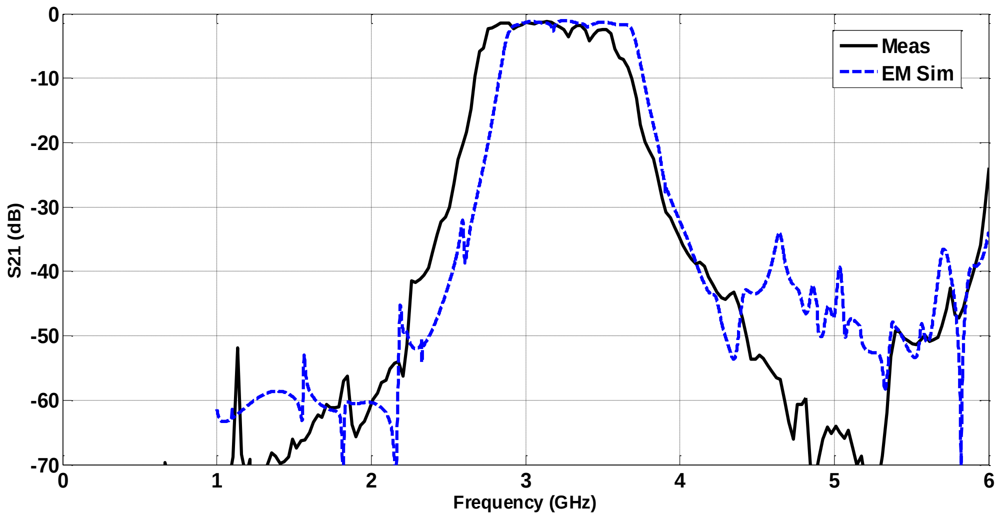


(a)

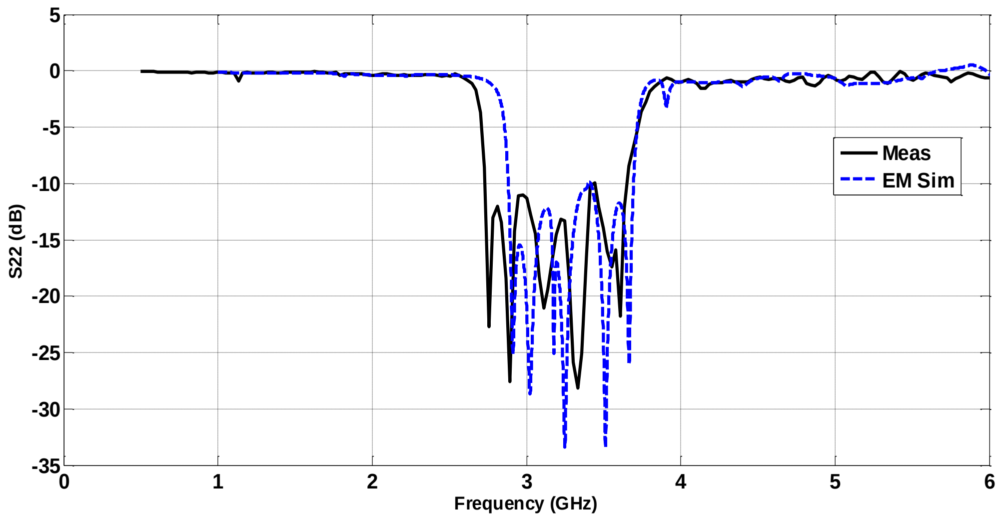


(b)

Figure 5.8: Measurements vs. EM simulation results of filter 2 in TX channel (a) S11 (b) S12.



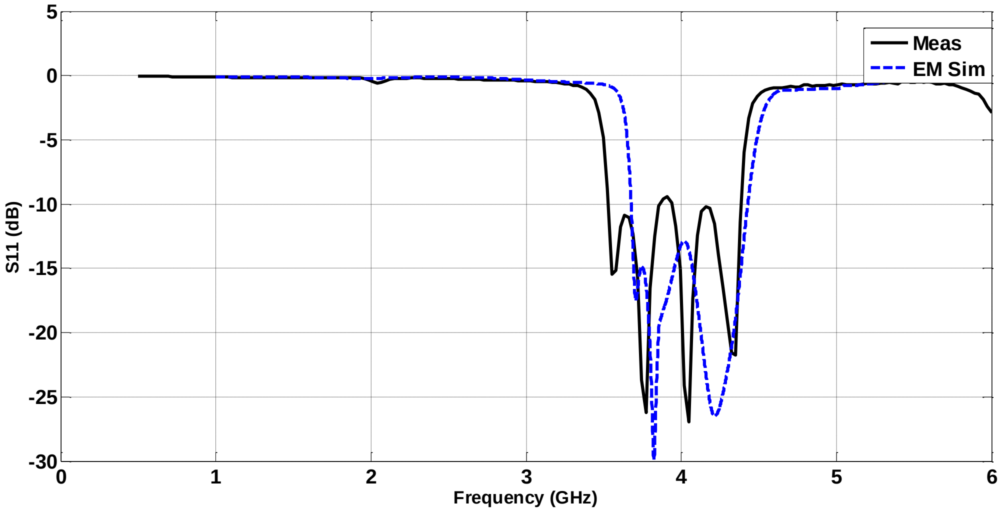
(a)



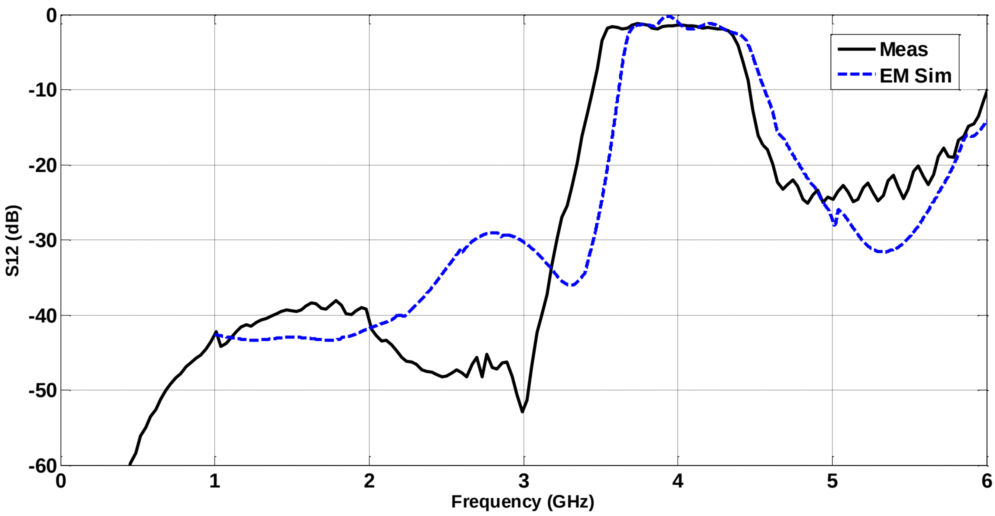
(b)

Figure 5.9: Measurements vs. EM simulation results of filter 2 in TX channel (a) S21 (b) S22.

LO Channel Filter 2: 3.80-4.40 GHz

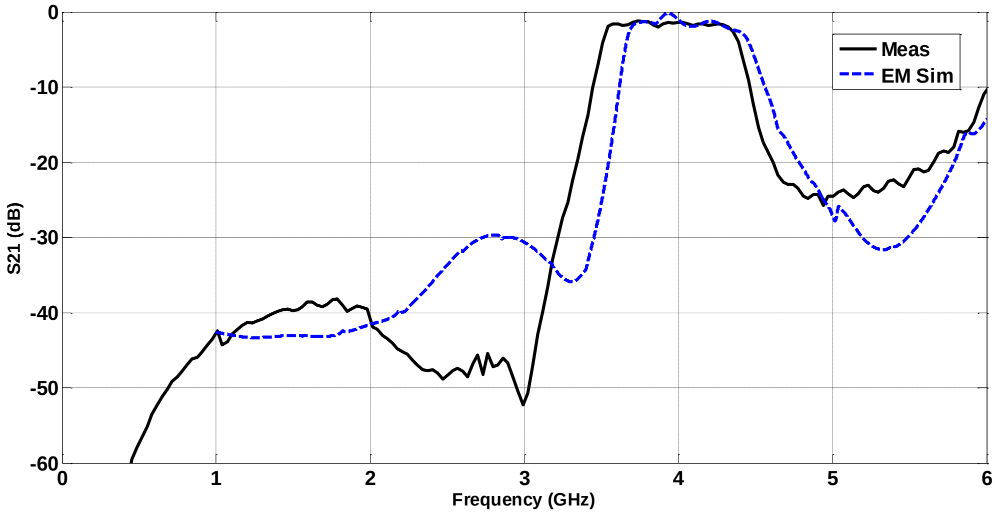


(a)

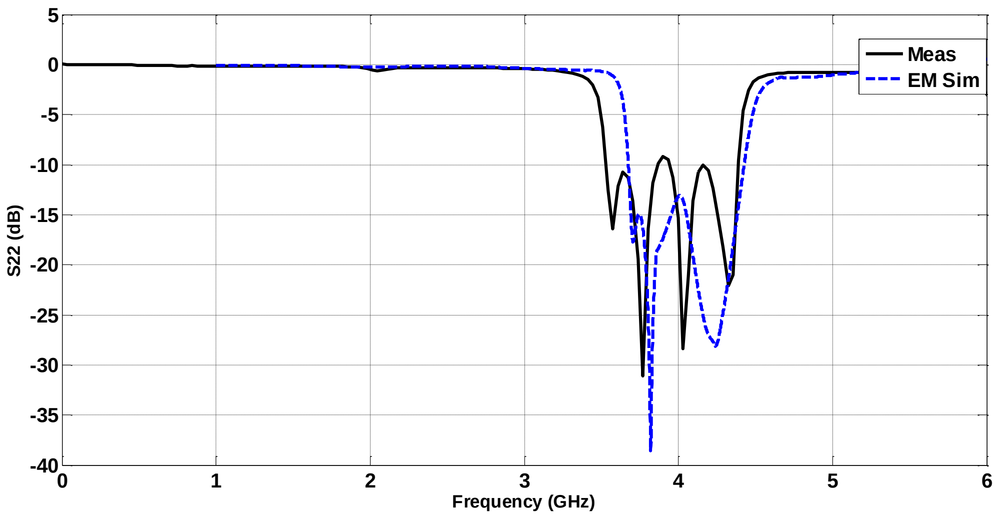


(b)

Figure 5.10: Measurements vs. EM simulation results of filter 2 in LO channel (a) S11 (b) S12.



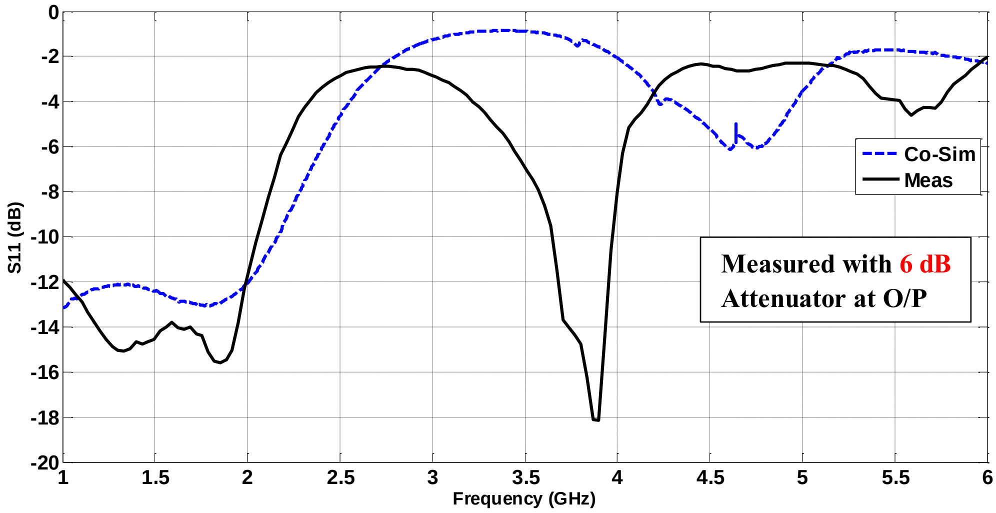
(a)



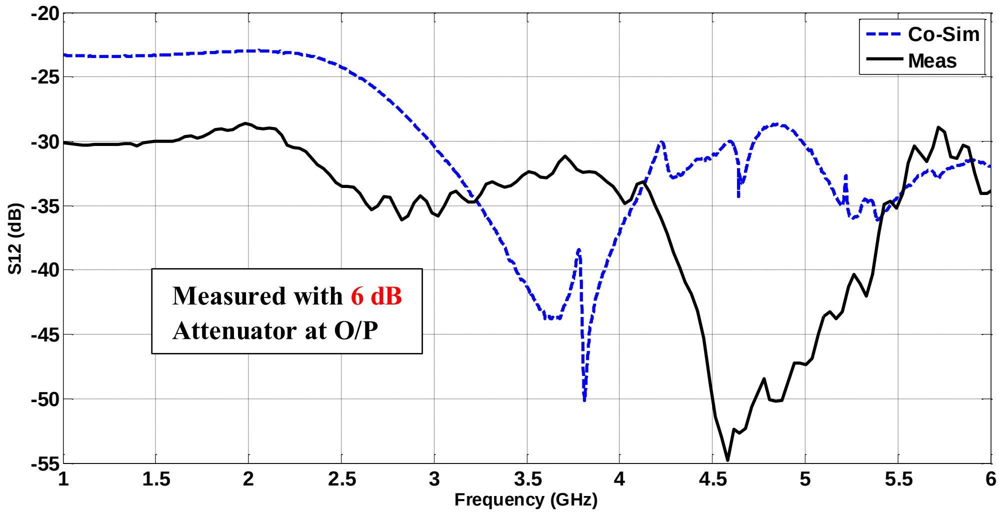
(b)

Figure 5.11: Measurements vs. EM simulation results of filter 2 in LO channel (a) S21 (b) S22.

<u>Amplifier 1 in TX channel (Q1): 1.52-1.82 GHz</u>

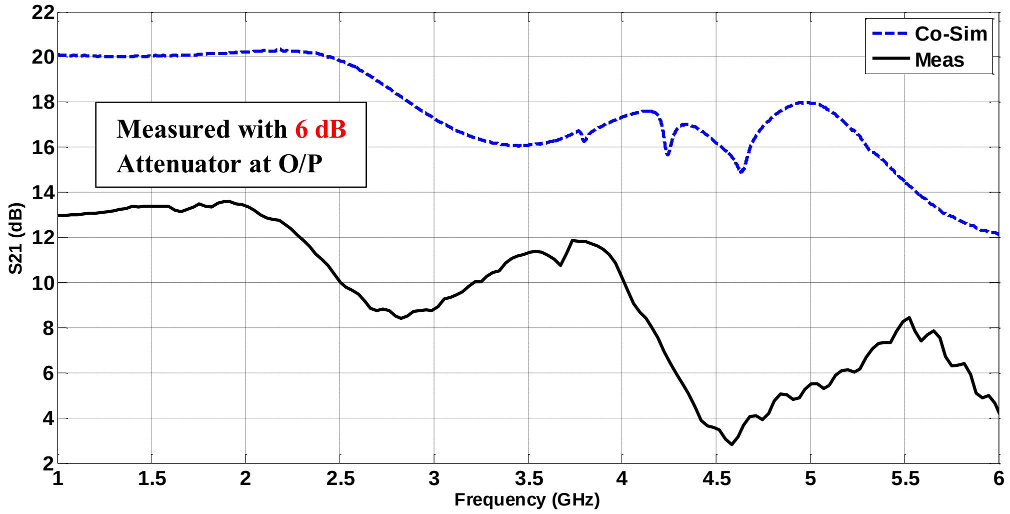


(a)

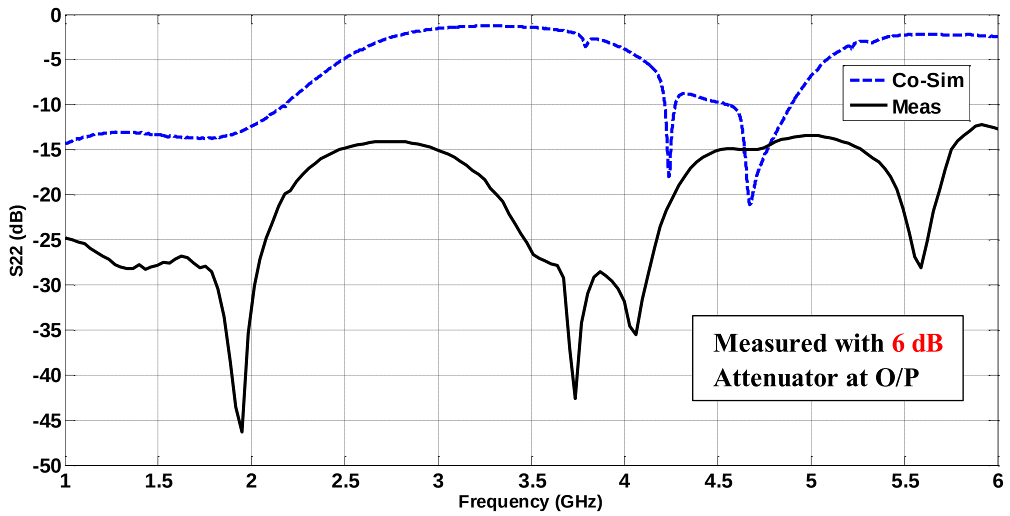


(b)

Figure 5.12: Measurements vs. co-simulation results of amplifier 1 in TX channel (a) S11 (b) S12.



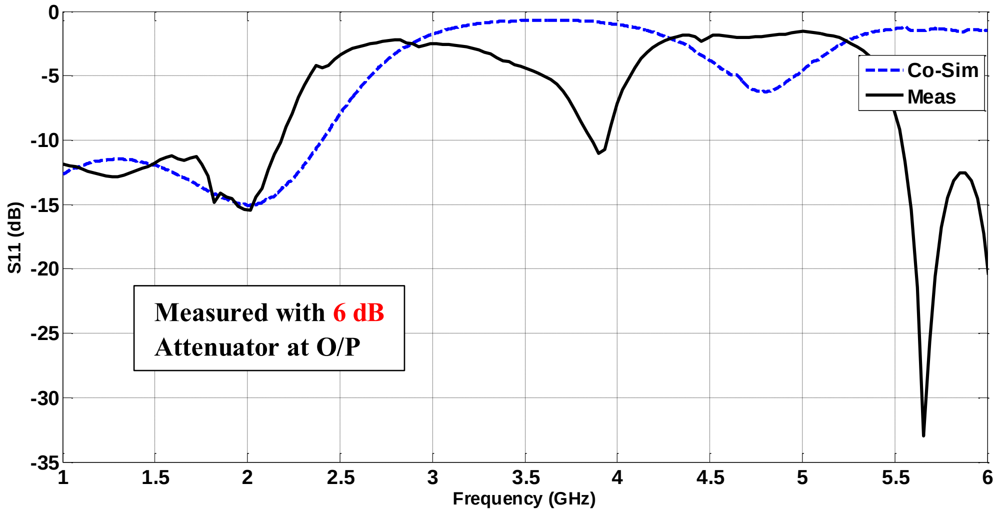
(a)



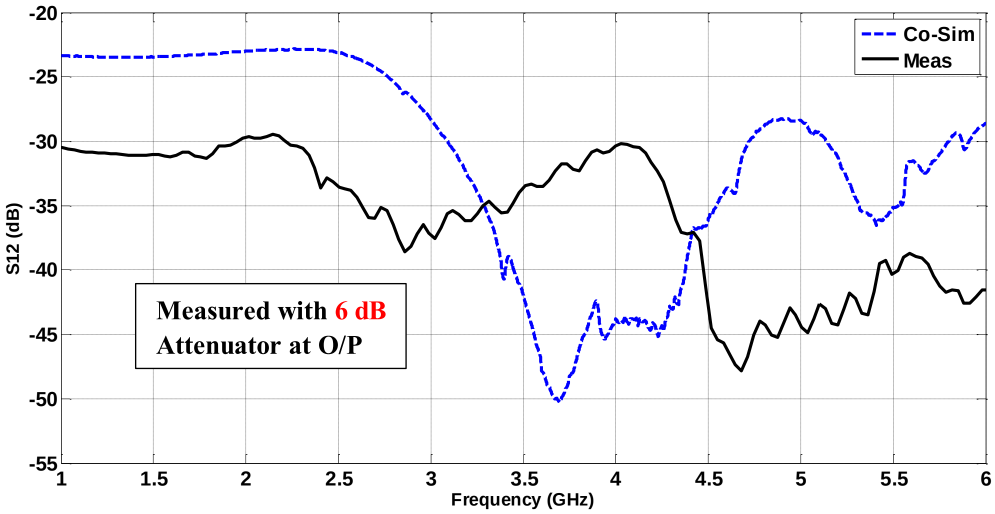
(b)

Figure 5.13: Measurements vs. co-simulation results of amplifier 1 in TX channel (a) S21 (b) S22.

Amplifier 1 in LO channel (Q3): 1.90-2.20 GHz

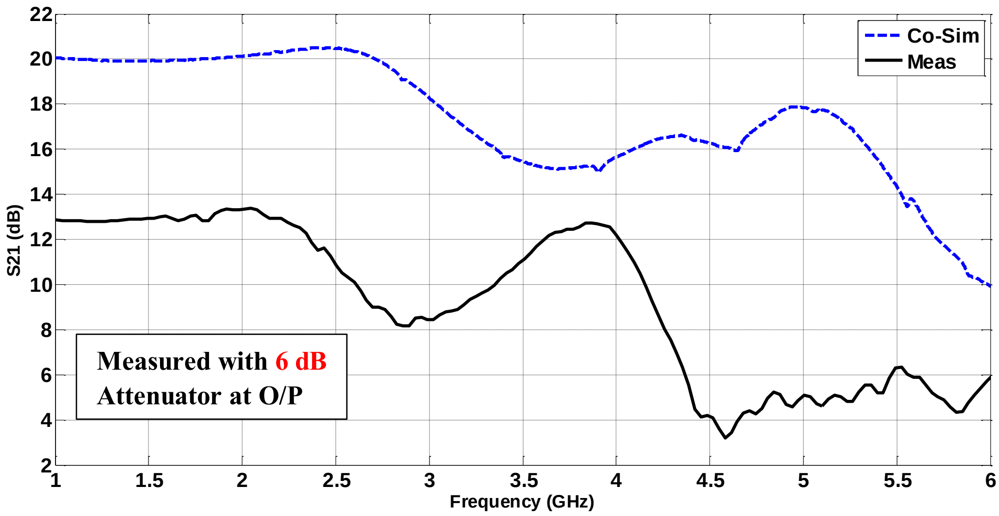


(a)

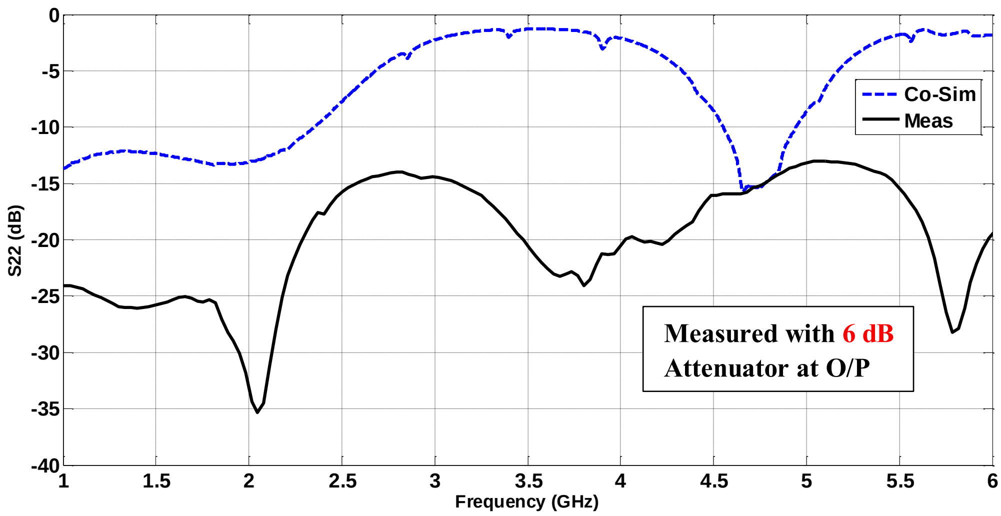


(b)

Figure 5.14: Measurements vs. co-simulation results of amplifier 1 in LO channel (a) S11 (b) S12.



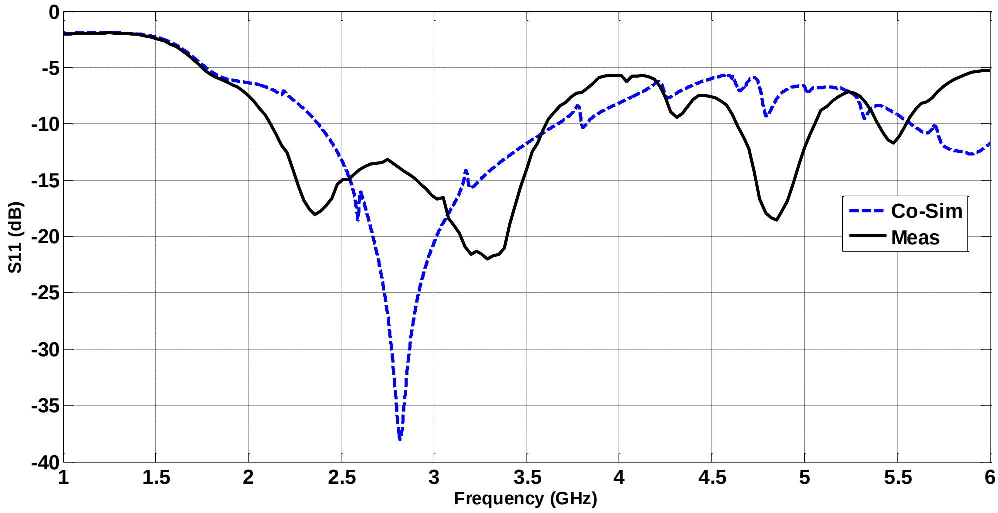
(a)



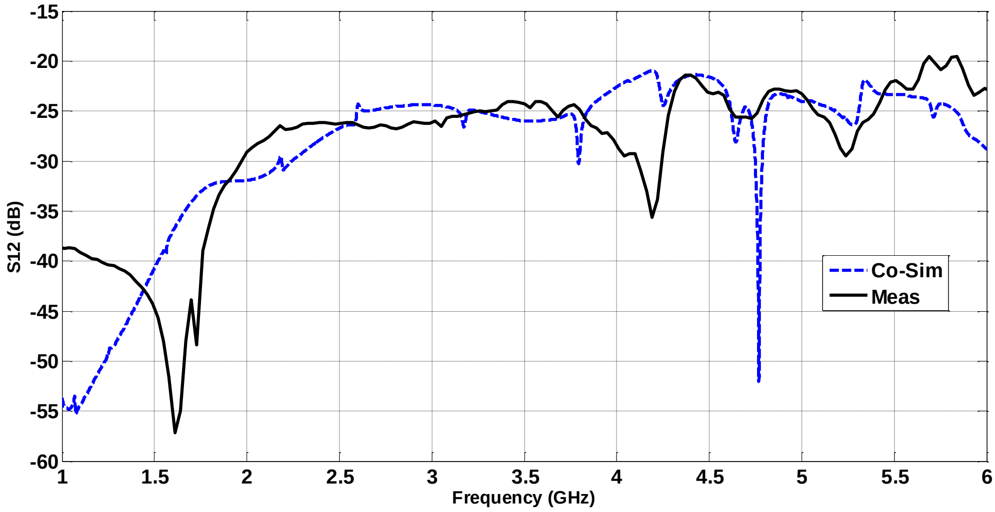
(b)

Figure 5.15: Measurements vs. co-simulation results of amplifier 1 in LO channel (a) S21 (b) S22.

Amplifier 2 in TX channel (Q2): 3.04-3.64 GHz

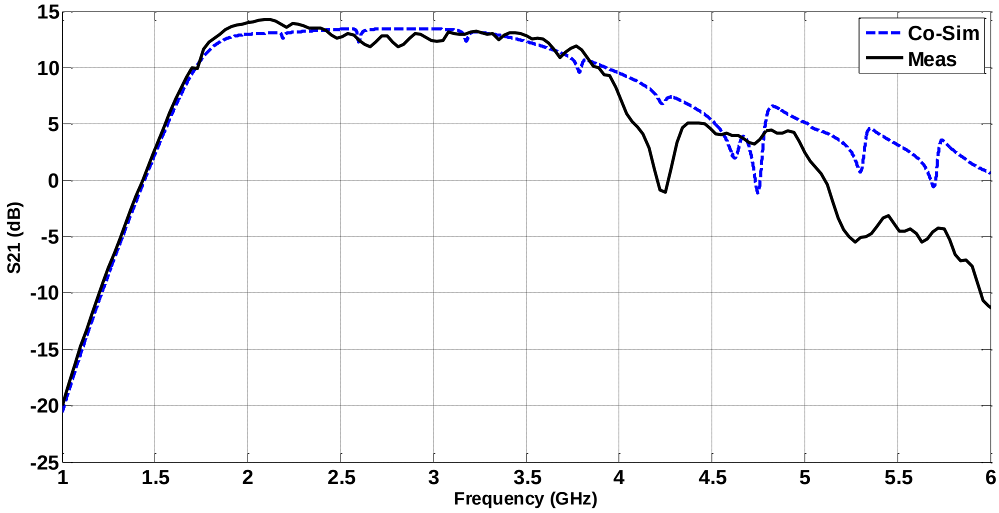


(a)

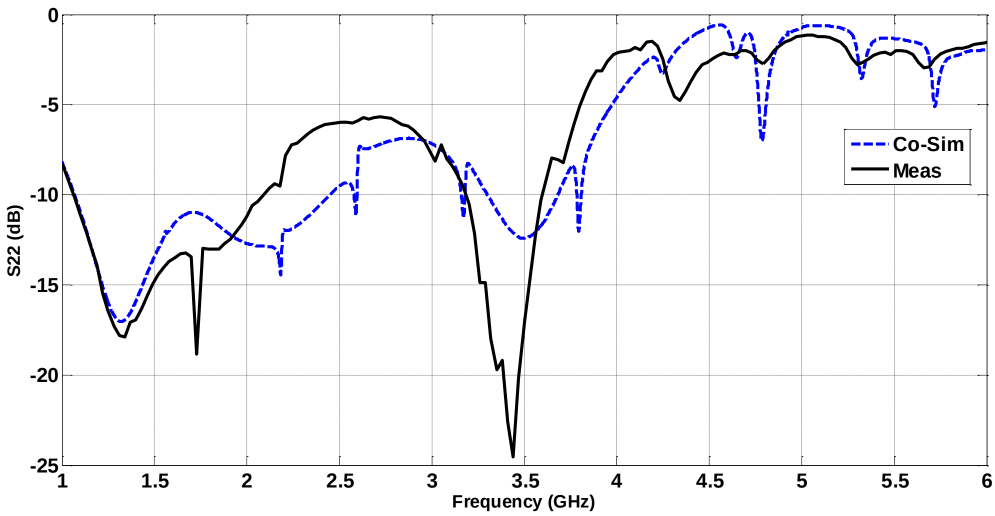


(b)

Figure 5.16: Measurements vs. co-simulation results of amplifier 2 in TX channel (a) S11 (b) S12.



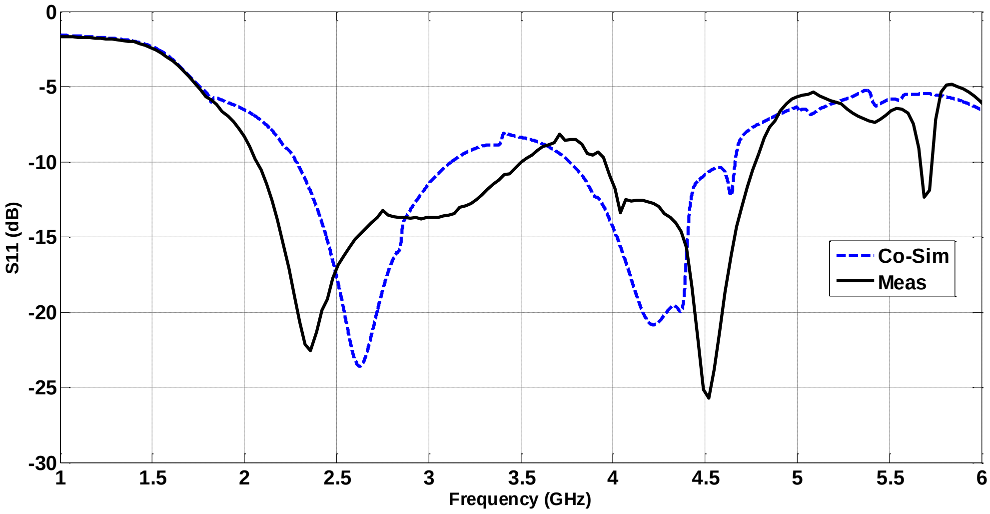
(a)



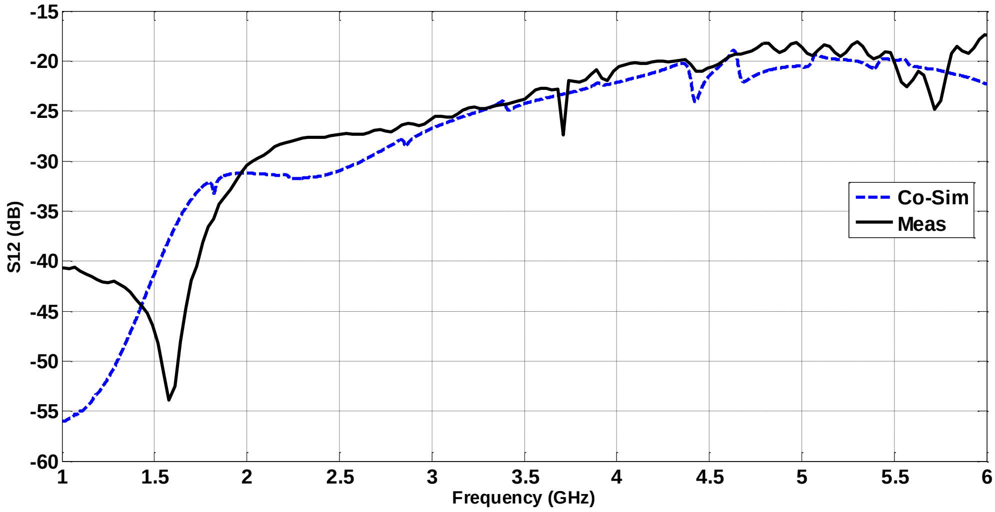
(b)

Figure 5.17: Measurements vs. co-simulation results of amplifier 2 in TX channel (a) S21 (b) S22.

<u>*Amplifier 2 in LO channel (Q4): 3.80-4.40 GHz*</u>

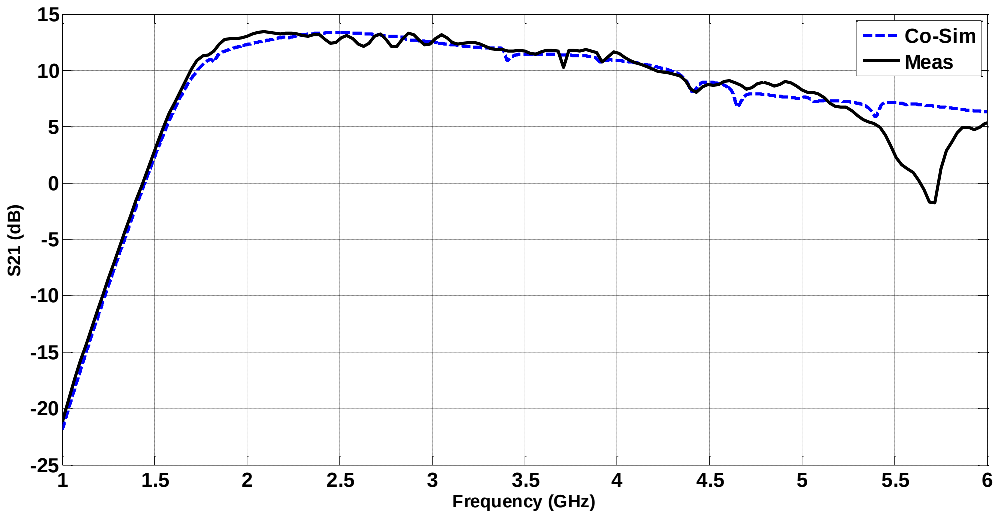


(a)

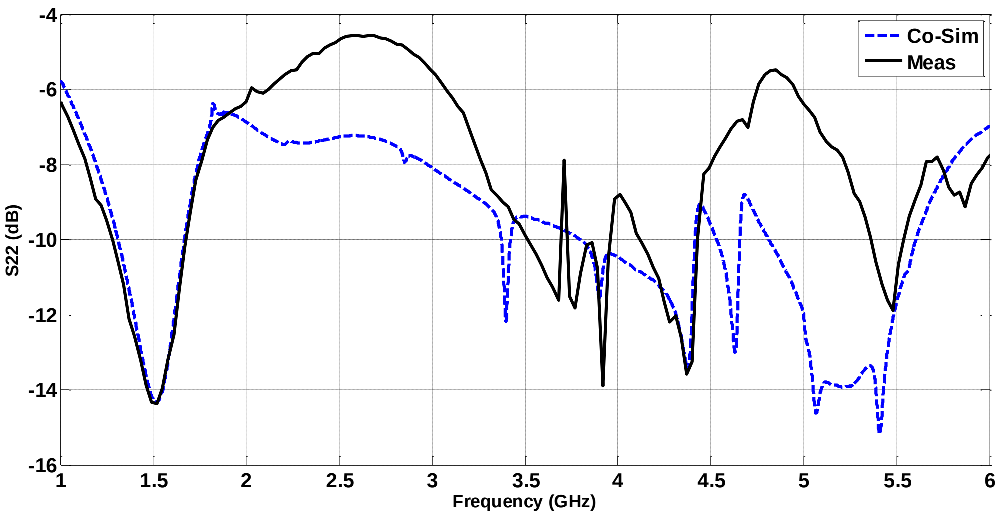


(b)

Figure 5.18: Measurements vs. co-simulation results of amplifier 2 in LO channel (a) S11 (b) S12.



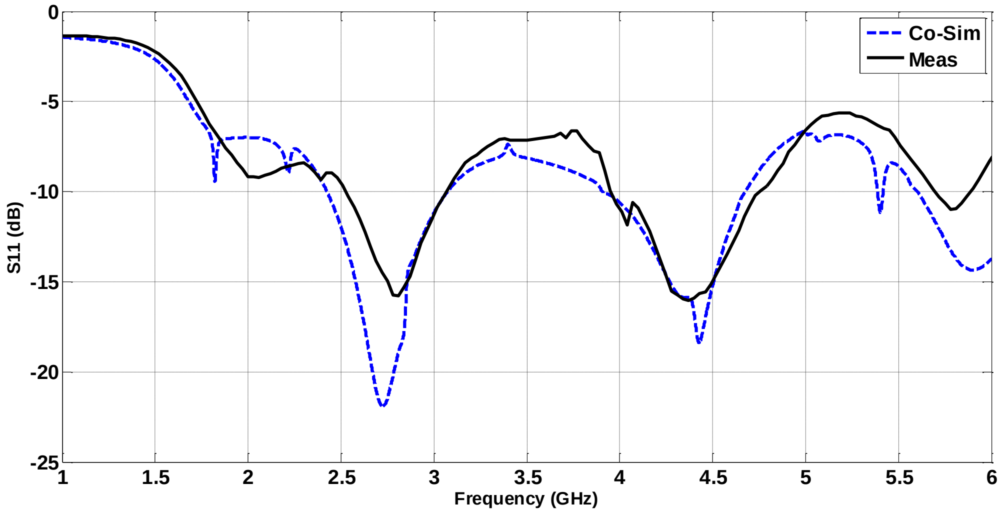
(a)



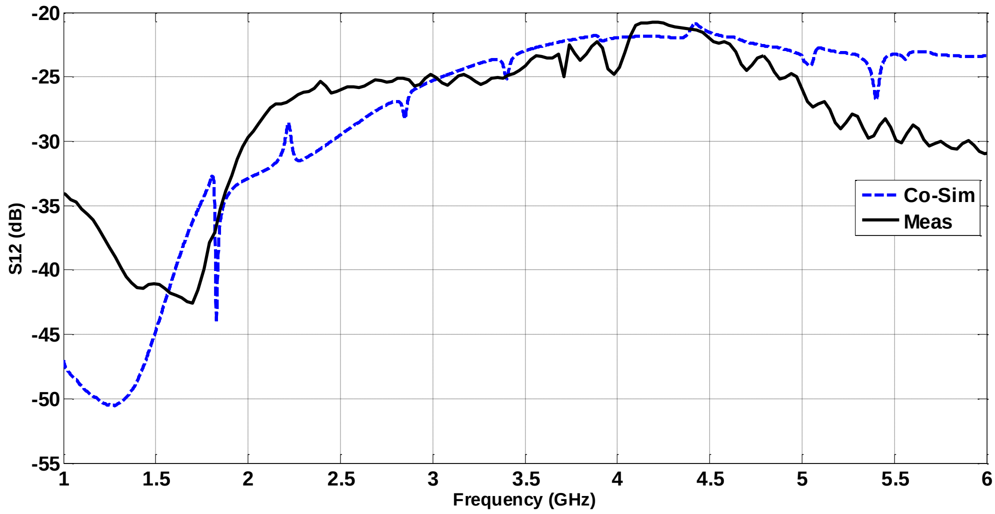
(b)

Figure 5.19: Measurements vs. co-simulation results of amplifier 2 in LO channel (a) S21 (b) S22.

Amplifier 3 in LO channel (Q5): 3.80-4.40 GHz

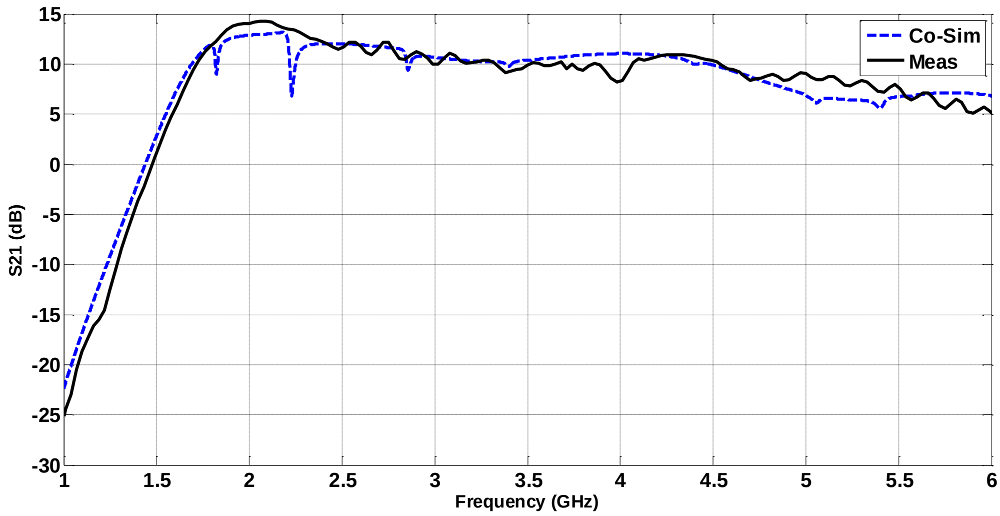


(a)

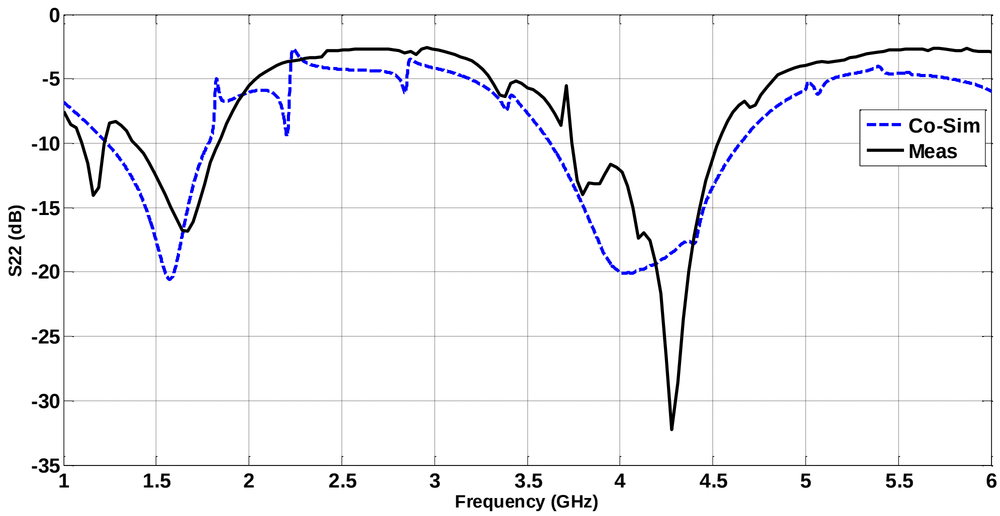


(b)

Figure 5.20: Measurements vs. co-simulation results of amplifier 3 in LO channel (a) S11 (b) S12.



(a)



(b)

Figure 5.21: Measurements vs. co-simulation results of amplifier 3 in LO channel (a) S21 (b) S22.

5.1.2 RX PCB

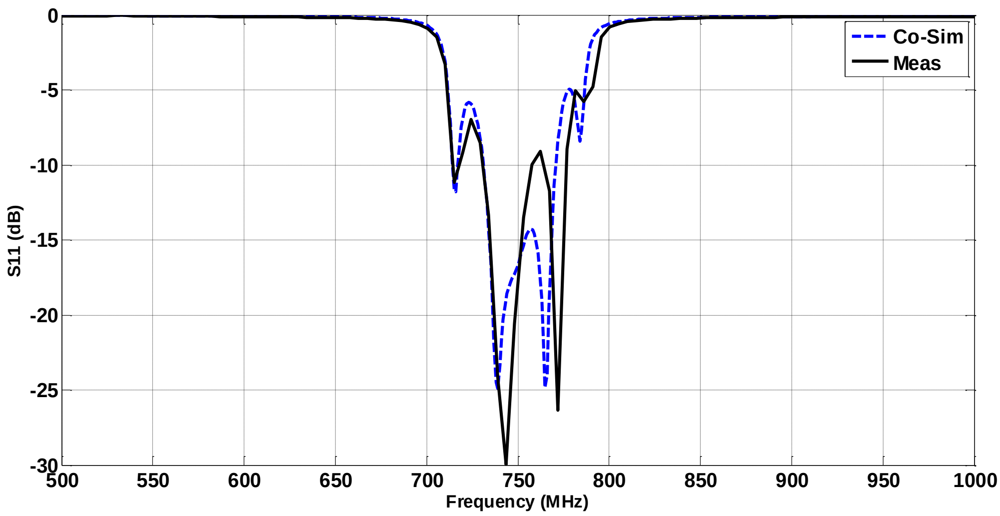
The RX PCB comprises two receiver channels which are replicas of each other. On the RX PCB, the BPF and the SBB1089Z amplifier of each down-conversion stage were cascaded. Hence, the reverse isolation (S12) responses of all stages should be an attenuated band pass response with negative magnitude (in dB). On the other hand, the gain (S21) responses of all stages should be an amplified version of the band pass response with positive magnitude (in dB). The input and output return loss of the cascaded stages should be more negative (in dB) as all the BPFs and amplifiers are matched to 50 Ω over the desired frequency bands. The test and measurements of the cascaded BPF and SBB1089Z amplifier of the two RX channels are discussed in the following session. The comparison of the S-parameter measurement of the RX channels along with the ADS co-simulation results of each cascaded stage are presented accordingly.

5.1.2.1 First Down-Converter Stage Filter – Amplifier (750-770 MHz)

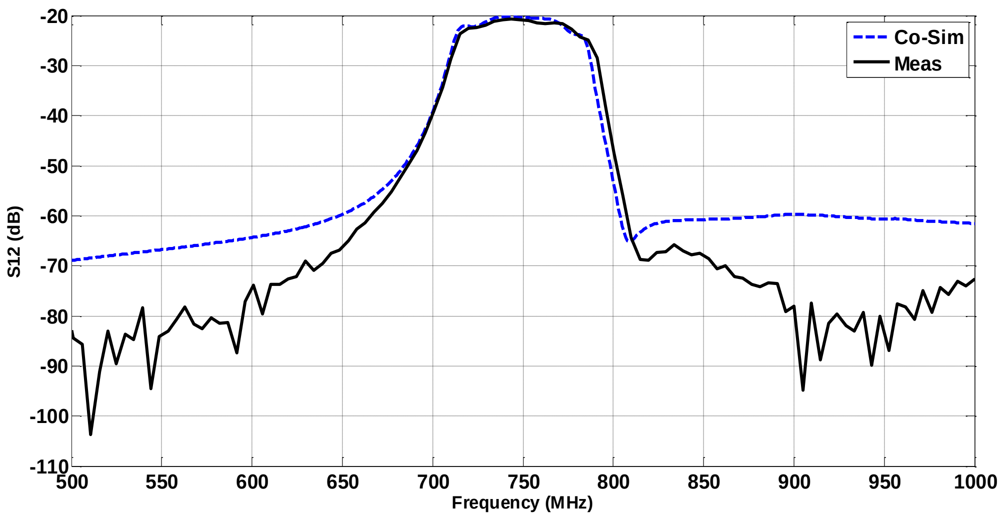
The measured S-parameter responses of the filter-amplifier of the first down-converter stage in both RX channels along with their ADS co-simulation responses are presented in Figure 5.22 – Figure 5.25. From these plots, a perfect match between the measured and simulation results is observed in the overall S-parameter responses. As it is seen, the input and output return losses of the first cascaded stages of both RX channels follow the expected simulation trends, indicating good impedance matching with the 50 Ω characteristic impedance of the system. The bandwidths of the filters along with the attenuation characteristics of the transmission and reverse isolations perfectly match with the simulation results, validating the accuracy and precision of the performed co-simulation along with the high quality fabrication.

5.1.2.2 Second Down-Converter Stage Filter – Amplifier (62-78 MHz)

The measured S-parameter responses of the filter-amplifier of the second down-converter stage in both RX channels along with their ADS co-simulation responses are depicted in Figure 5.26 – Figure 5.29. From these graphs, a perfect match between the measured and simulation results is observed in the overall S-parameter responses. As it is seen, the input and output return losses of both RX channels follow the expected simulation trends, indicating good impedance matching with the 50 Ω characteristic impedance of the system. The bandwidths of the filters along with the rejection characteristics of the transmission and reverse isolations perfectly match with the simulation results. The measured S21 and S12 responses show a 100% match between the measured and simulation results from the low frequencies up to 150 MHz. This validates the accuracy as well as the precision of the performed ADS co-simulation along with the high quality fabrication.

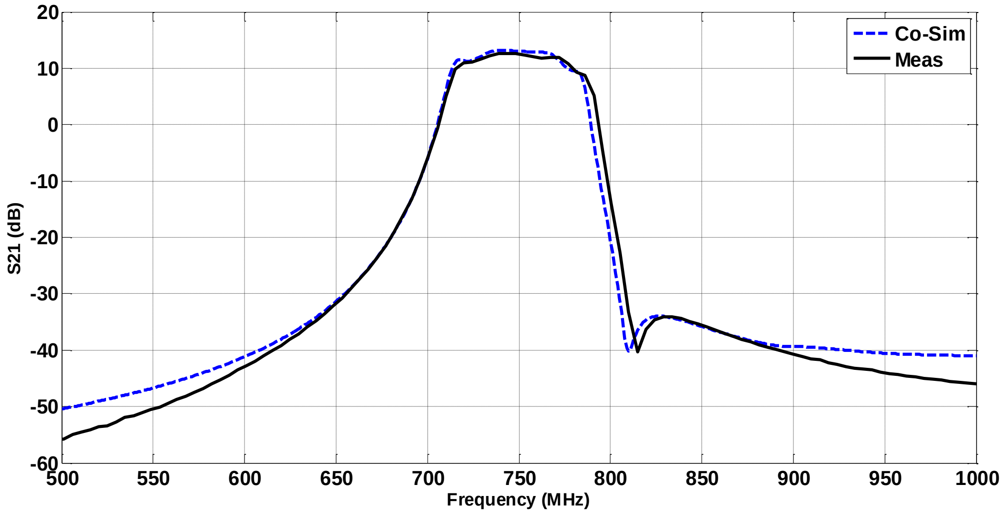


(a)

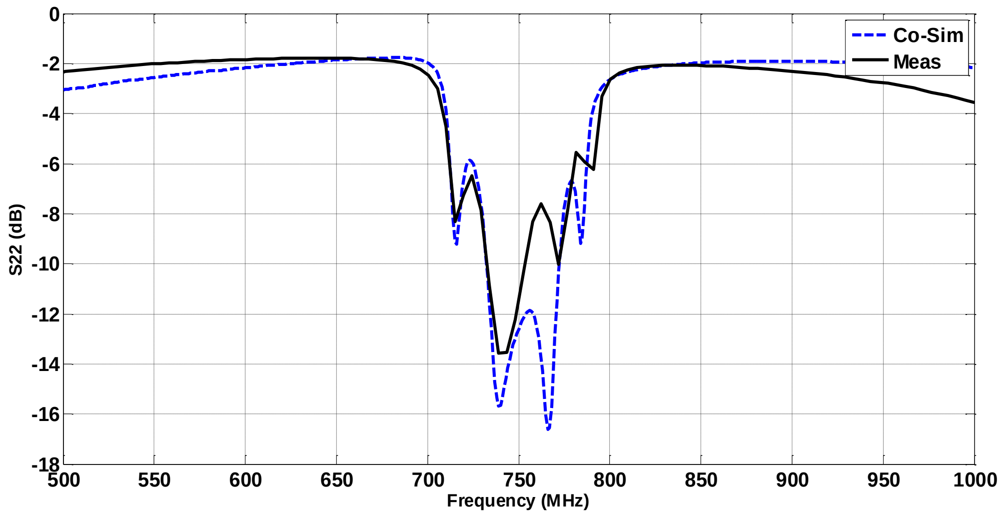


(b)

Figure 5.22: Measurements vs. co-simulation results of RX 1 channel filter – amplifier 1, Q11 (a) S11 (b) S12



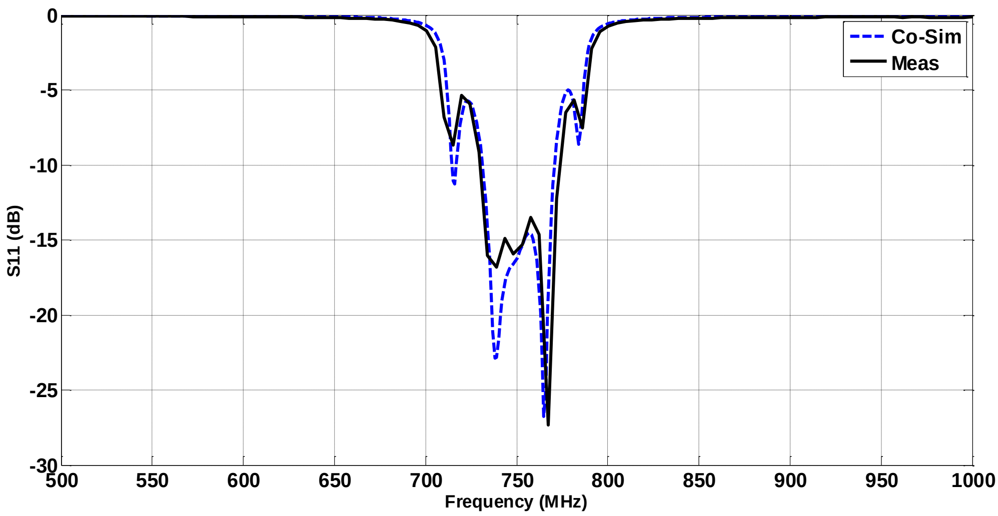
(a)



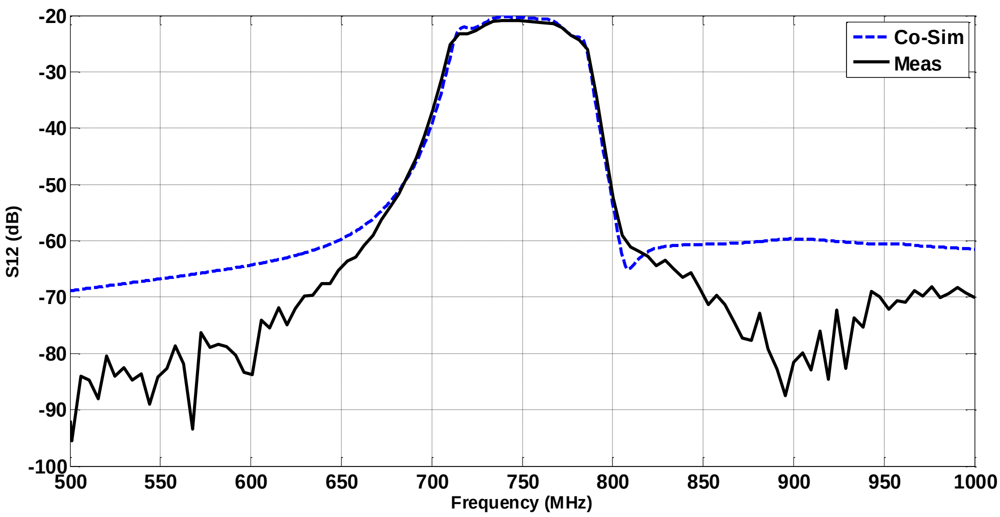
(b)

Figure 5.23: Measurements vs. co-simulation results of RX 1 channel filter – amplifier 1, Q11 (a) S21 (b) S22.

RX 2 channel filter – amplifier 1 (Q21)

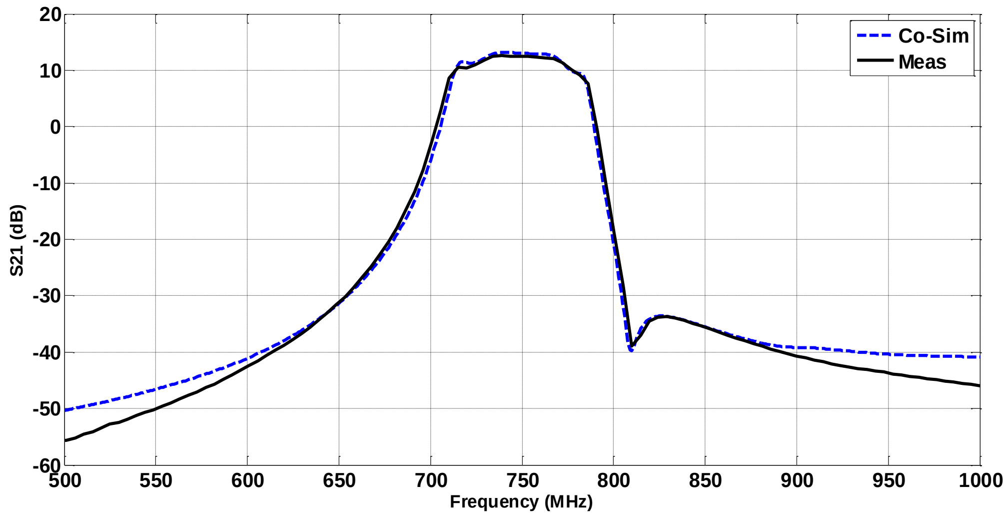


(a)

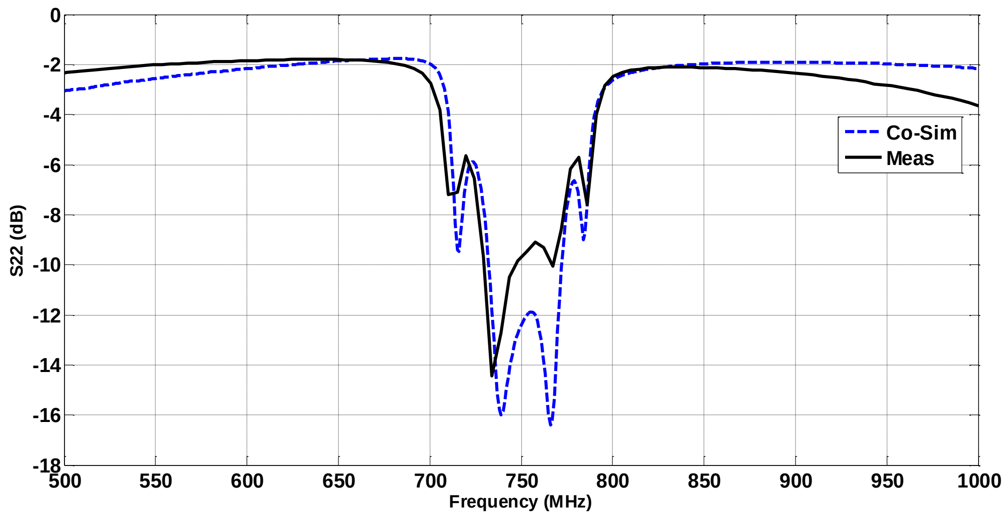


(b)

Figure 5.24: Measurements vs. co-simulation results of RX 2 channel filter – amplifier 1, Q21 (a) S11 (b) S12.



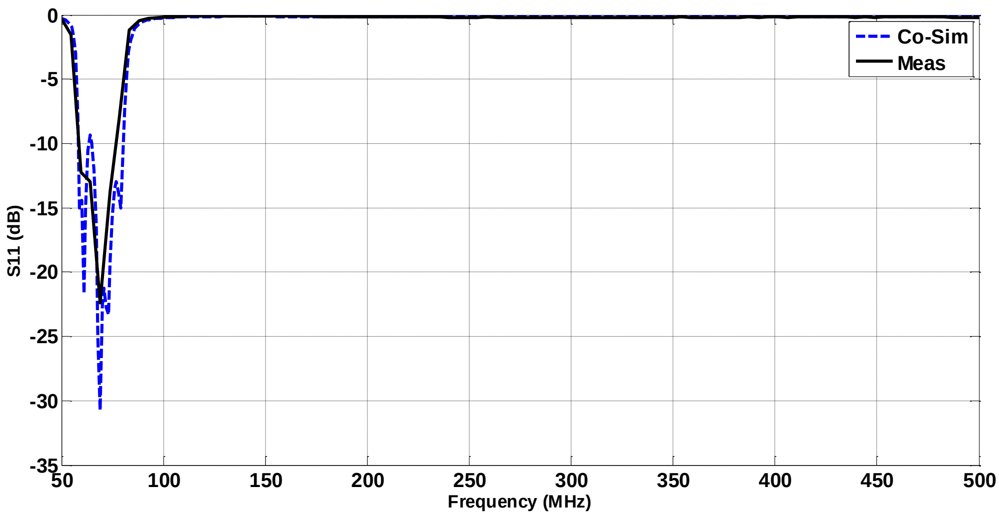
(a)



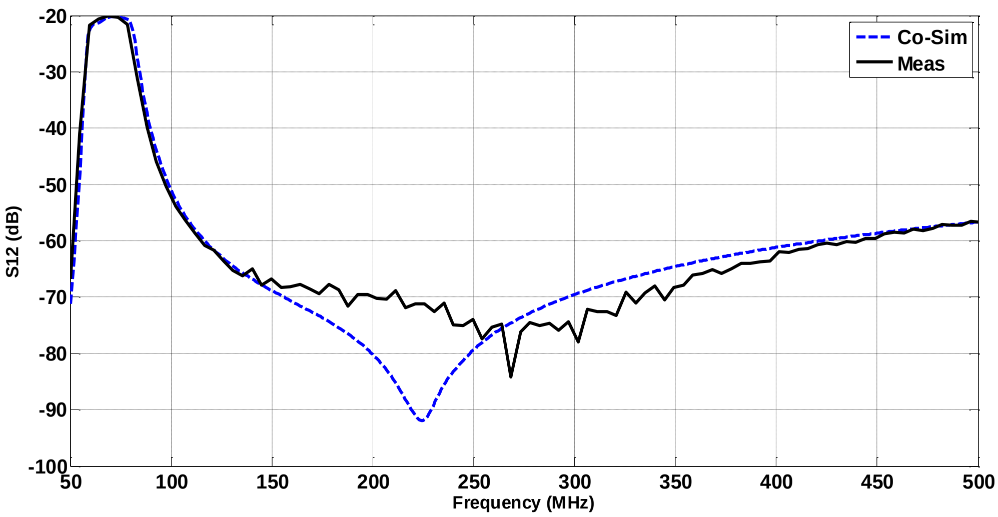
(b)

Figure 5.25: Measurements vs. co-simulation results of RX 2 channel filter – amplifier 1, Q21 (a) S21 (b) S22.

RX 1 channel filter – amplifier 2 (Q12)

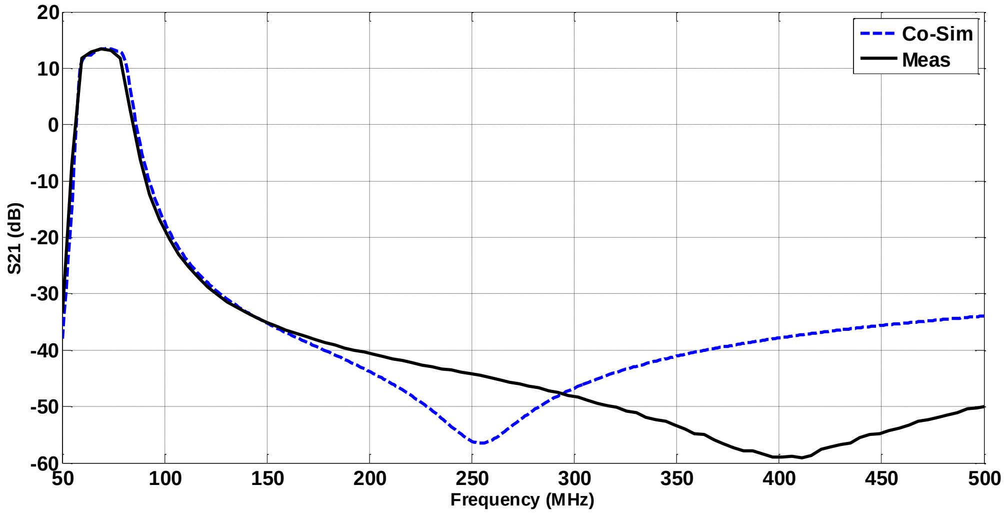


(a)

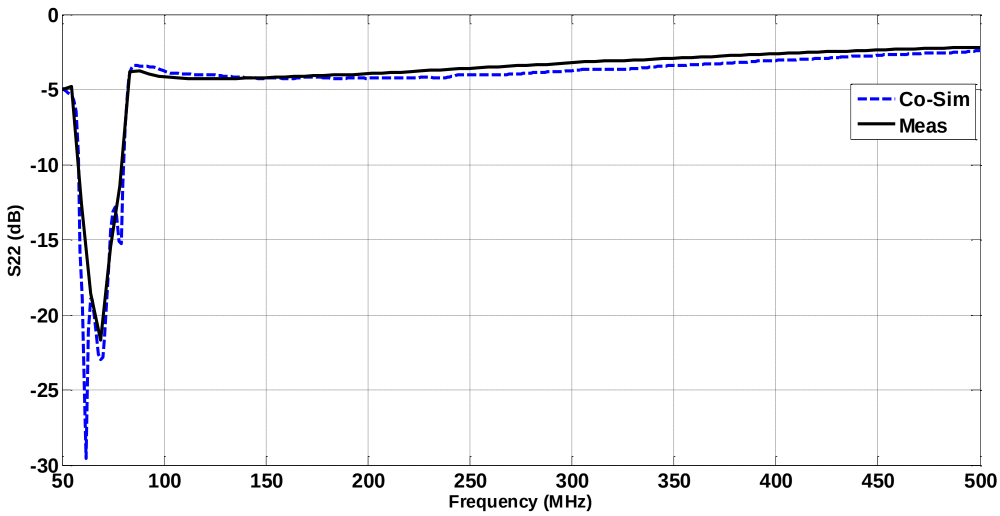


(b)

Figure 5.26: Measurements vs. co-simulation results of RX 1 channel filter – amplifier 2, Q12 (a) S11 (b) S12.



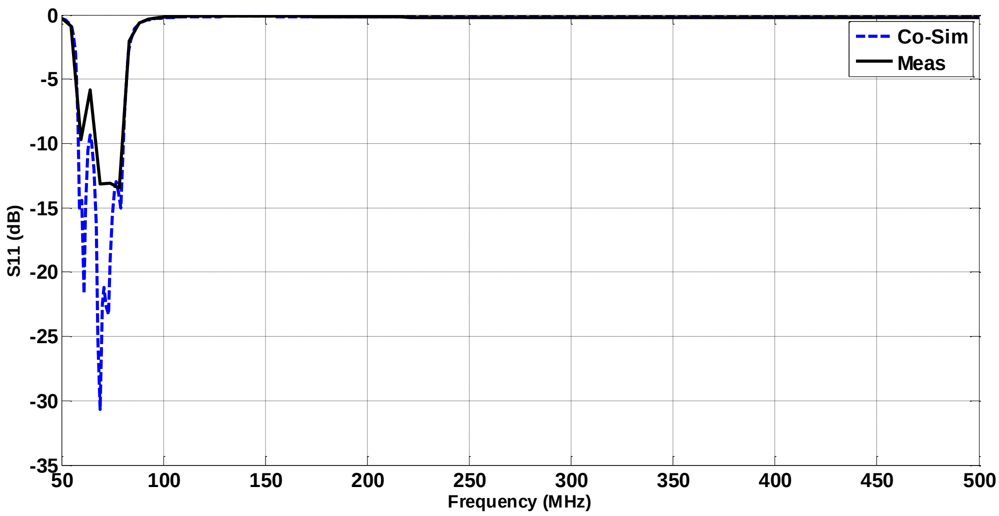
(a)



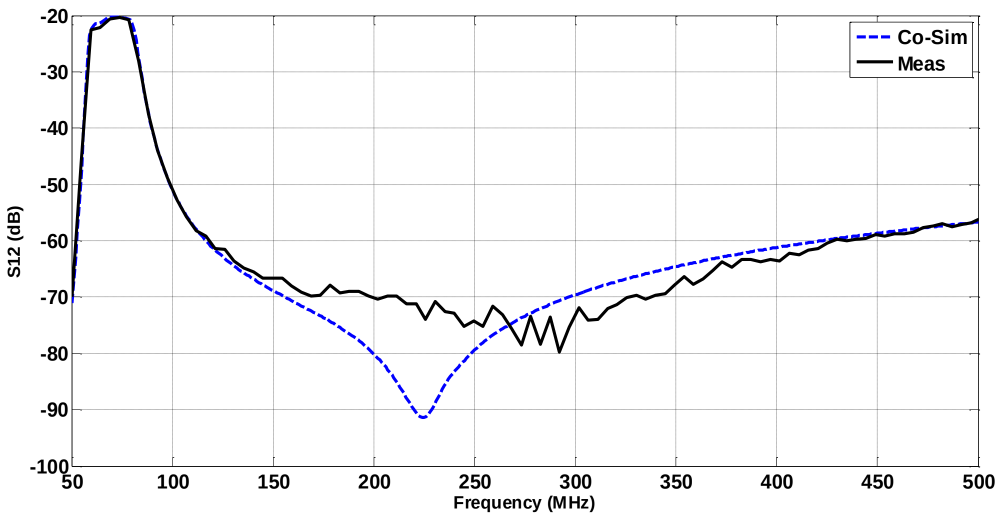
(b)

Figure 5.27: Measurements vs. co-simulation results of RX 1 channel filter – amplifier 2, Q12 (a) S21 (b) S22.

<u>*RX 2 channel filter – amplifier 2 (Q22)*</u>

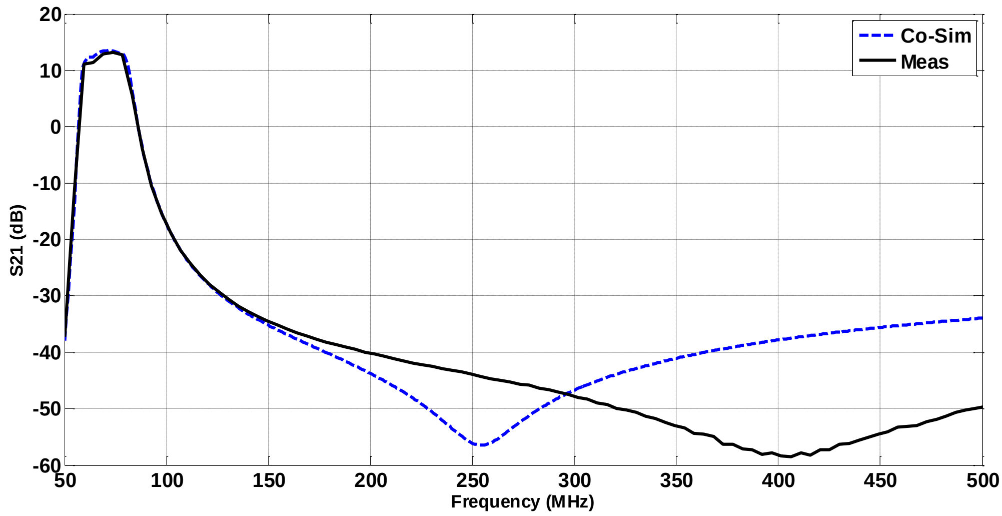


(a)

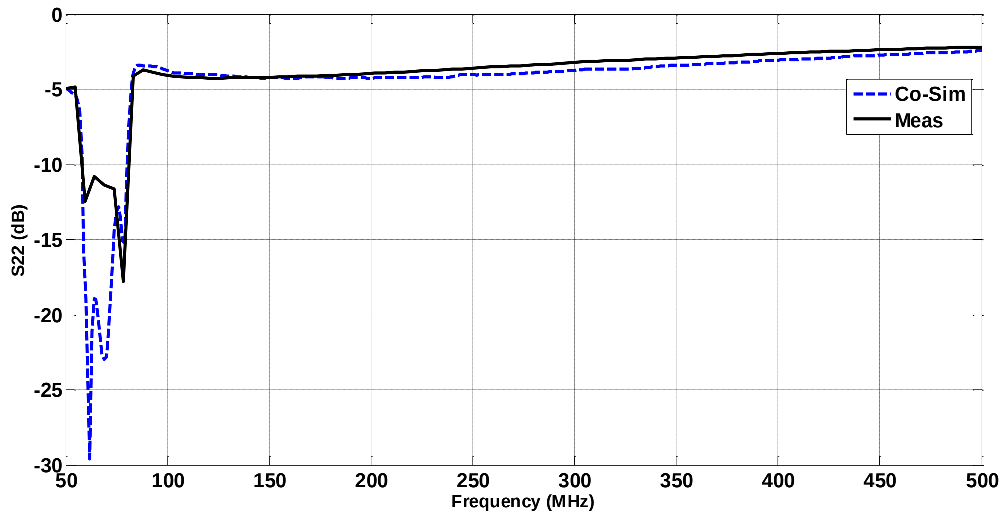


(b)

Figure 5.28: Measurements vs. co-simulation results of RX 2 channel filter – amplifier 2, Q22 (a) S11 (b) S12.



(a)



(b)

Figure 5.29: Measurements vs. co-simulation results of RX 2 channel filter – amplifier 2, Q22 (a) S21 (b) S22.

5.2 Measurements vs. Simulations of Radar's PCB Testbed

This section presents the simulation and practical tests of the overall miniaturized radar system on PCB. First, the result of AWR system simulation with the ADS simulated S-parameter responses of individual stages is discussed. Then, the measurement setups and results of the fabricated radar PCBs with single tone and wideband LFM chirp inputs are presented.

5.2.1 AWR System Simulation with S-Parameters of Individual Stages

By simulating the individual BPF and amplifier stages in ADS, the S-parameter responses of those stages were extracted as two-port networks in Touchstone file format (.S2P). The Touchstone files were imported in the AWR simulator to verify the functionality of the overall radar system integrated on the PCBs. Initially, the overall system was tested by applying a single tone input at 350 MHz (the center frequency of the desired band) and the signal power at the output of different stages of the TX, LO, and RX channels were monitored. These simulated output power levels were close to the calculated values in the spreadsheet calculations.

The output spectrum of the simulated miniaturized radar testbed with an LFM chirp input signal from 200-500 MHz is shown in Figure 5.30. This input chirp results in 600 MHz instantaneous bandwidths for the TX and LO channels. As it is shown, a strong tone is received at 70 MHz with an approximate in-band dynamic range of 60 dB. The simulated out-of-band dynamic range is approximately 100 dB which indicates a good filtering at the receiver channel. The response of the last stage filter of the receiver is obvious around the in-band frequencies.

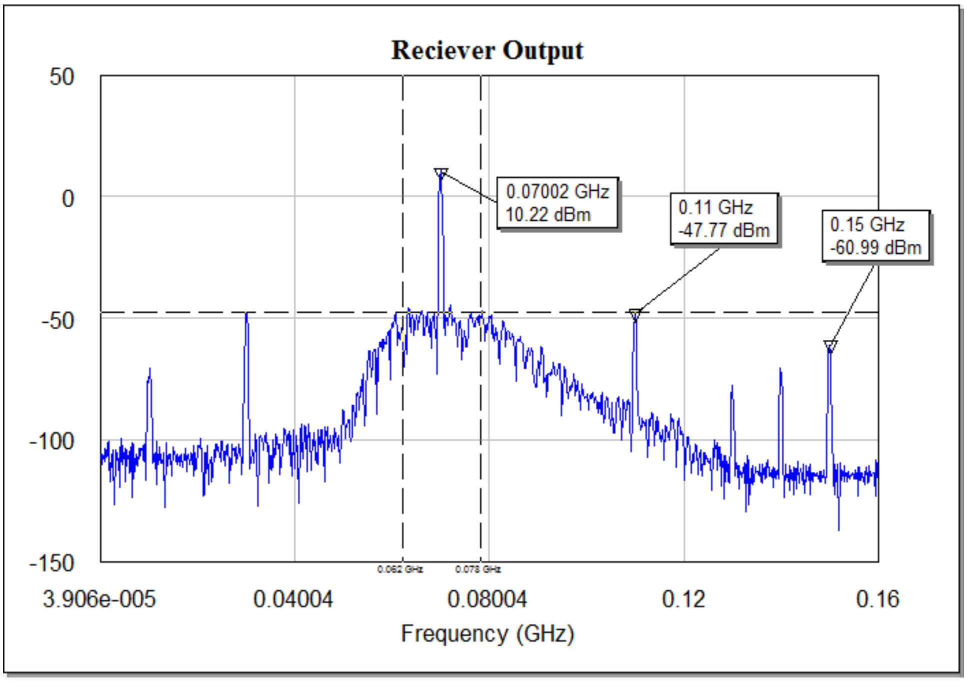


Figure 5.30: Miniaturized digital radar output with the simulated S-parameters of individual stages.

5.2.2 PCB Testbed Measurements with Single Tone Input Signal

After verifying the responses of the individual amplifiers and BPFs versus the simulated ones, the fabricated boards were ready to be examined at a system level. For the first system experiment, the outputs of the fabricated TX, LO, and RX channels were examined using a single tone at 350 MHz. The measurement setup of the following experiment is shown in Figure 5.31, accordingly. This experimental setup consists of RF signal synthesizers (1 – 3 GHz) to generate the required baseband signals for the inputs as well as to drive the on-board mixers of each channel, a power supply to provide the required DC supply to the on-board amplifiers, and a VNA spectrum analyzer (DC – 6 GHz) to measure the output spectrum of each channel.

The measured output spectrum of the fabricated TX, LO, and RX channels with single tone input are shown in Figure 5.32 – 5.34, respectively. As expected from the system calculations and simulations in Chapter 2, the up-converted signal at the output of the TX channel is a single tone signal at 3.34 GHz with a power level of 7.4 dBm. The filtering of this channel is perfect as there are no other frequency components in the measured spectrum. Also, the up-converted output of the LO channel is at 4.1 GHz with a power level of 10.2 dBm. The measured power level is good enough to drive the first stage's down-converter mixer of the receiver channel into nonlinearity. The only downside of the measured output spectrum of the LO channel is the leakage of its fundamental frequency at 2.05 GHz to the output of the channel. Nevertheless, the power level of this harmonic is attenuated to -21.4 dBm by the second stage BPF of the LO channel. This is lower compared to the power level of the wanted signal. However, a higher order filter with higher rejection at 2.05 GHz could solve the leakage of this fundamental frequency at the mixer stage to the output of the LO channel. The output of the RX channel is measured by feeding the TX and LO channels to the first down-conversion stage, which resulted in a 5 dBm tone at 70 MHz. Other harmonics of the fundamental frequency such as 140 MHz are present at the output of the RX channel spectrum. These out-of-band harmonics do not affect the performance of the digital radar testbed and were expected from the AWR system simulations in Chapter 2.

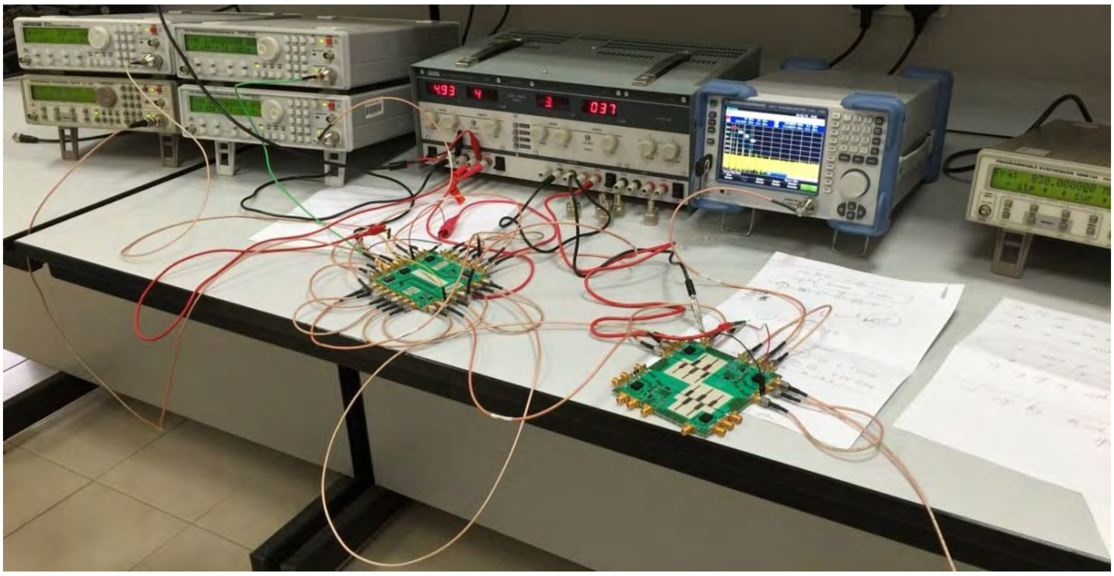


Figure 5.31: Measurement setup for single tone input signal.

Figure 5.32: Output spectrum of fabricated TX channel with single tone input signal.

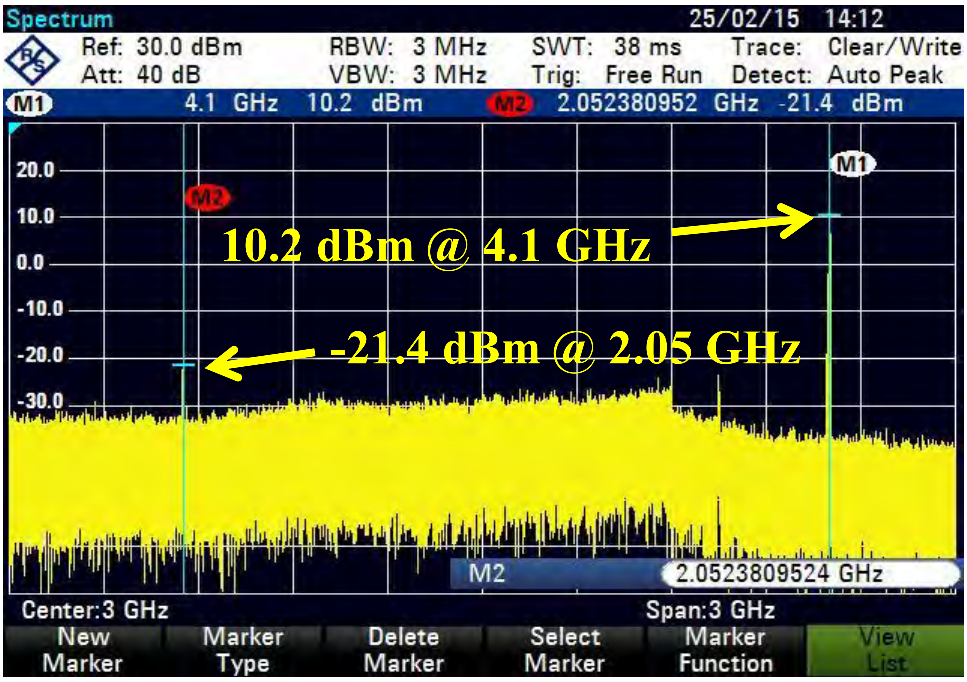


Figure 5.33: Output spectrum of fabricated LO channel with single tone input signal.

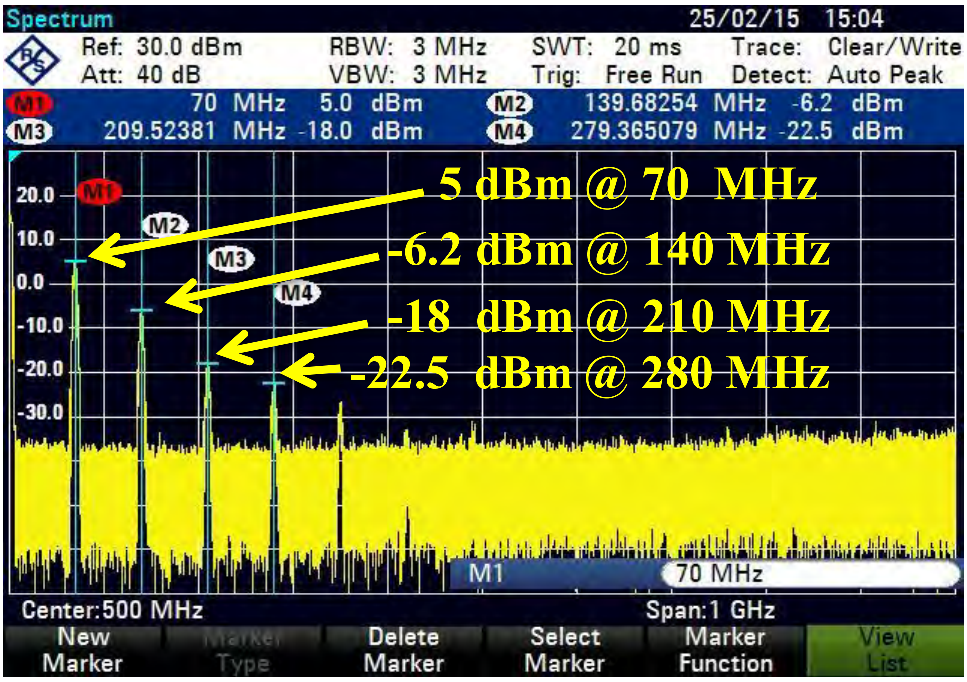


Figure 5.34: Output spectrum of fabricated RX channel with single tone input signal.

5.2.3 PCB Testbed Measurements with Wideband Input Signal (LFM Chirp)

By evaluating the performance of the miniaturized digital radar testbed using a single tone input signal, the PCBs were ready to be examined over a wideband input signal and measure the output of the receiver using ADC. Figure 5.35 depicts the experimental setup to verify the overall dynamic range of the miniaturized radar testbed on the PCB. Similar to the large-scale radar testbed evaluation in Chapter 2, the experimental setup consists of RF signal synthesizers (1 – 3 GHz) to generate the required drive tones for the on-board mixers of each channel, a power supply unit to provide the required DC supply for the on-board amplifiers, an Agilent M9331A AWG (with 10-bit resolution and 1.25 GS/S) to generate the required LFM chirp input signals for the TX and LO channels, and an Agilent M9210A ADC (with 10-bit resolution and 2 – 4 GS/S) to digitize the output signal of the RX channel. The digitized output of ADC was displayed on a soft-front-panel, displayed on the monitor in Figure 5.35.

The output of the miniaturized digital testbed radar for different LFM chirp input signals with 100 MHz and 300 MHz instantaneous bandwidths are depicted in Figure 5.36 and Figure 5.37, respectively. As the output frequency corresponds to the range resolution of the stretch processed system, the digitized output is displayed in the frequency domain. The instantaneous bandwidths of the up-converted chirps at the output of the TX and LO channels are 200 MHz and 600 MHz, respectively for the two experimental cases. These correspond to range resolutions of 0.75 m and 0.25 m, respectively. For both cases, a strong tone signal is present at 70 MHz in the range profiles of the radar testbed and a high in-band dynamic range of 80 dB and 75 dB is achieved, respectively. In comparison, the generated out-of-band harmonics as well as the noise floor are increased when the system is excited with a wider bandwidth signal. However, the achieved out-of-band dynamic range is high enough not to disrupt the process and analysis of the radar's range profile.

From the measured results for the LFM chirp of 200-500 MHz, 75 dB in-band and 82 dB out-of-band dynamic ranges are achieved for a 0.25 m range resolution. The achieved high dynamic range infers that all the components of the miniaturized radar testbed designed on the PCB operate in the linear region over the entire intended frequency range. Hence, the signal powers at the input of all stages are well below their P1dB compression points which reduce the generated system's IMDs (nonlinearity) and prevent system saturation. These results provide solid proof of the undertaken frequency plan of the miniaturized digital radar testbed for PCB. In addition, the implemented filters show proper rejection of the undesired frequency bands, as per their design, at all stages of the radar system. A comparison of the key performance characteristics of the miniaturized digital radar testbed alongside the previous digital radar testbed using discrete microwave components is given in Table 5.1.

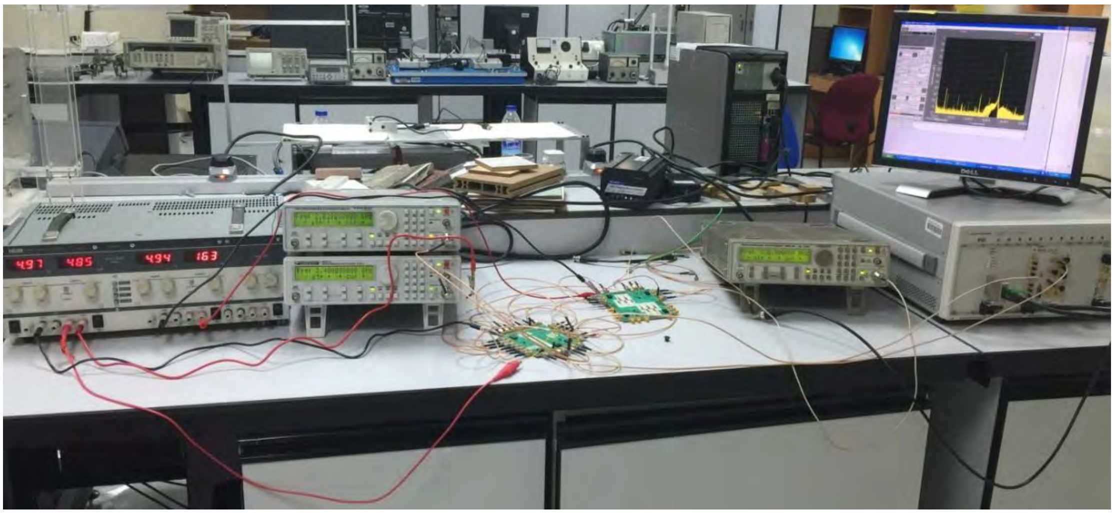


Figure 5.35: Measurement setup for wideband LFP chirp input signal with ADC.

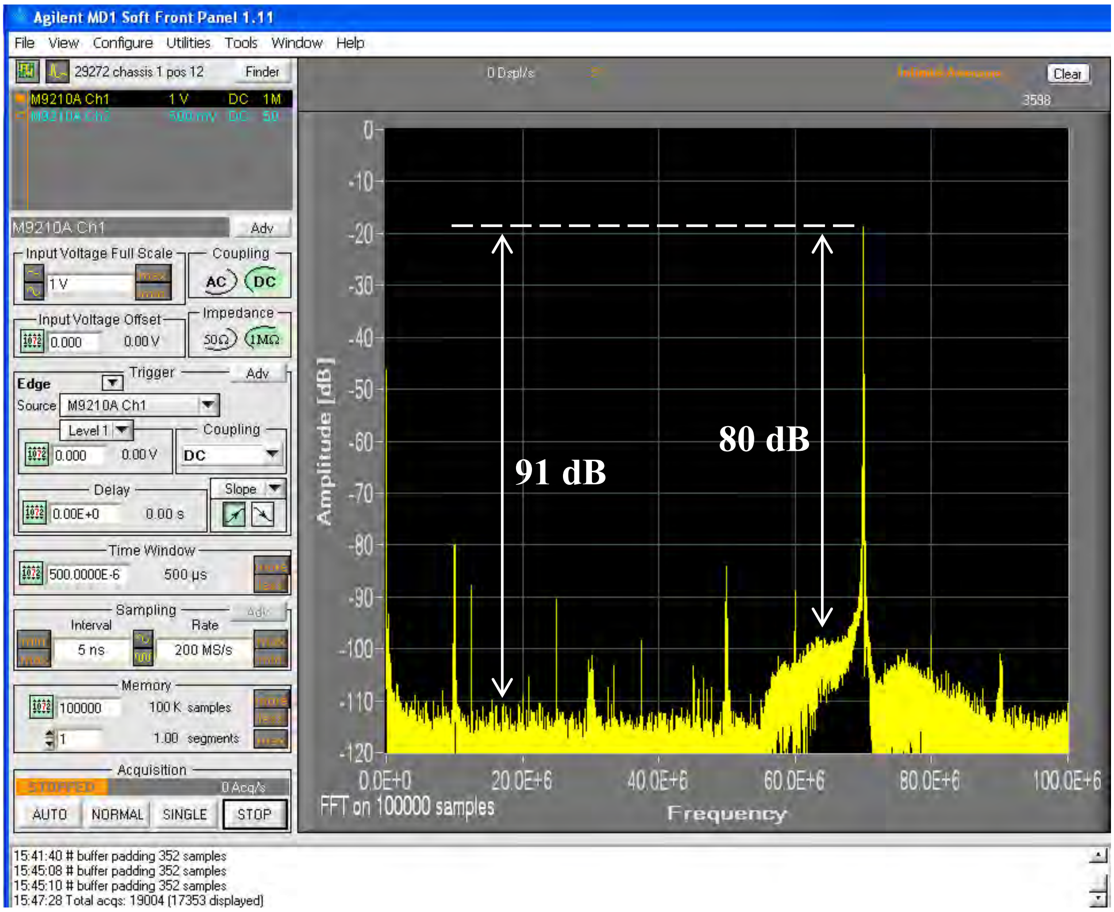


Figure 5.36: Output of the fabricated digital radar testbed for LFM chirp input (300-400 MHz); 200 MHz instantaneous bandwidth.

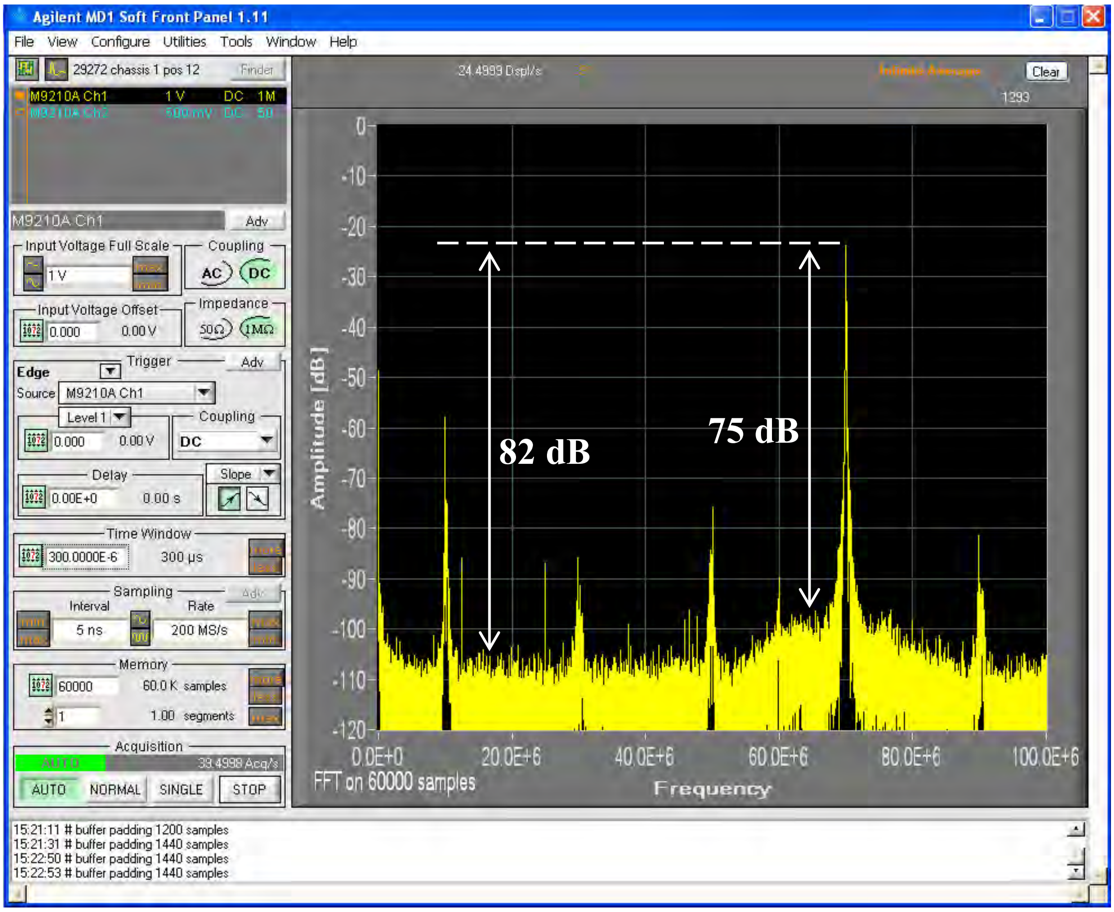


Figure 5.37: Output of the fabricated digital radar testbed for LFM chirp input (200-500 MHz); 600 MHz instantaneous bandwidth.

Table 5.1: Characteristics of miniaturized digital radar on PCB vs. digital radar with discrete microwave components.

Specification	**Digital radar testbed – Microwave components**	**Digital radar testbed – PCB**
Frequency (TX Channel)	3040 – 3640 MHz	3040 – 3640 MHz
Frequency (LO Channel)	3800 – 3400 MHz	3800 – 3400 MHz
Bandwidth	600 MHz	600 MHz
Number of Receivers	2	2
In-Band Dynamic Range	60 dB	75 dB
Out-of-Band Dynamic Range	90 dB	82 dB
IF Frequency	70 MHz	70 MHz
IF Bandwidth	16 MHz	16 MHz
Size	Large	Small
Cost	High	Low
Portability	No	Yes

Chapter 6: Conclusions and Future Work

6.1 Conclusions

In this thesis, a portable, miniaturized, low-cost, and high-performance digital radar testbed is implemented on PCB. The radar system consists of novel transmitter and receiver architectures and utilizes the stretch processing technique for simultaneous high range resolution and high dynamic range in digital radars. In addition, it comprises multiple receiver channels which enable several techniques such as adaptive beamforming and spatial filtering. By transforming the extracted range profile of the targets into the digital domain, the presented digital radar testbed is able to perform digital filtering and digital signal processing in addition to the storage and offline processing of data. The presented measurement results of the overall radar testbed on the PCB show a high in-band dynamic range of 75 dB and out-of-band dynamic range of 82 dB for 600 MHz instantaneous bandwidth, which corresponds to 0.25 m of range resolution. Hence, a better performance of the digital radar is achieved compared to the larger-scale radar testbed using discrete microwave components, while reducing the physical size and overall cost of the system. The measurement results of the fabricated PCBs have not yet been reported in the literature for such small-scale digital radar testbeds.

In order to implement the miniaturized digital radar testbed, a fully cascaded RF system study was conducted. This study was conducted using a purpose built spreadsheet calculations for RF systems' definitions and the specifications of the available off-the-shelf surface mount components. The RF budget simulation of the ADS software was used to ensure the validity and reliability of the calculated systems' parameters obtained from the spreadsheet analysis. Moreover, the system architecture was simulated in the AWR software to test the overall system response under single tone and wideband LFM chirp input excitations. The presented system simulation results predicted the linear operation of different stages in the radar testbed's chain. The anticipated filters effectively rejected the generated IMDs which resulted in achieving a system with the required high dynamic range. The simulated results agreed well with the measurement results of the fabricated radar testbed on PCBs.

In order to reduce the overall cost of the system fabrication, the required BPFs for the transmitter and receiver channels were designed and simulated using microstrip technology. This eases the fabrication and integration of the designed filters with other electronic circuitries such as amplifiers, mixers, and frequency doublers and results in lowering the overall fabrication and assembly costs. The designed BPFs have different center frequencies and operation bandwidths. They fall into different categories which are parallel coupled line, hairpin, and interdigital filters for the transmitter channels and capacitively coupled types for the receiver channels. The measured results of the fabricated filters agreed well with the simulated results of full-wave EM simulations in ADS. Furthermore, the input and output impedances of the utilized amplifiers were matched to the system's characteristic impedance (50 Ω) over the frequency bands of interest. This was done in order to reduce interconnect impedance mismatch problems and avoid signal reflections. In order to calculate the power loss in the PCB due to the substrate and conductors, the developed layout of the radar testbed was simulated using co-simulation of ADS. The simulated results of different stages were imported into the AWR system simulation and the system was deemed functional.

6.2 Future Work

Further suggested improvements to the system include increasing the operational bandwidth of the system and increasing the number of receiver channels in order to enhance the radars' range resolution and adaptive beamforming capabilities, respectively. Furthermore, the system requires integration with wideband antennas in order to transmit and receive the required wideband signals.

The fabricated PCBs are designed to ease the testing of individual blocks in the system chain. With the proved functionality, the system could be further miniaturized by cascading several stages without the need for additional I/O paths. In addition to the reduction of the cascaded noise figure of the system, higher-order filters could enhance the overall dynamic range of the system. The overall noise figure of the system could be reduced by slight modification of the front ends by using LNAs. Due to the transmitter PCB's high frequency of operation, proper shielding between different circuits is recommended for future fabrication. The overall system could be miniaturized further by chip level integration.

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Vita

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